

# *Power modules for E-vehicles – available solutions and future challenges*

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14 juni 2018  
1931 Congresscentrum Den Bosch

**POWER**  
**ELECTRONICS**

2018

# Key design objectives for Power Modules

## 1. Increase Power Density per package

- Chip technology → lower  $V_{CEsat}$
- Contacting technology within the power module → lower  $R_{thJC}$ , higher  $T_{jop}$

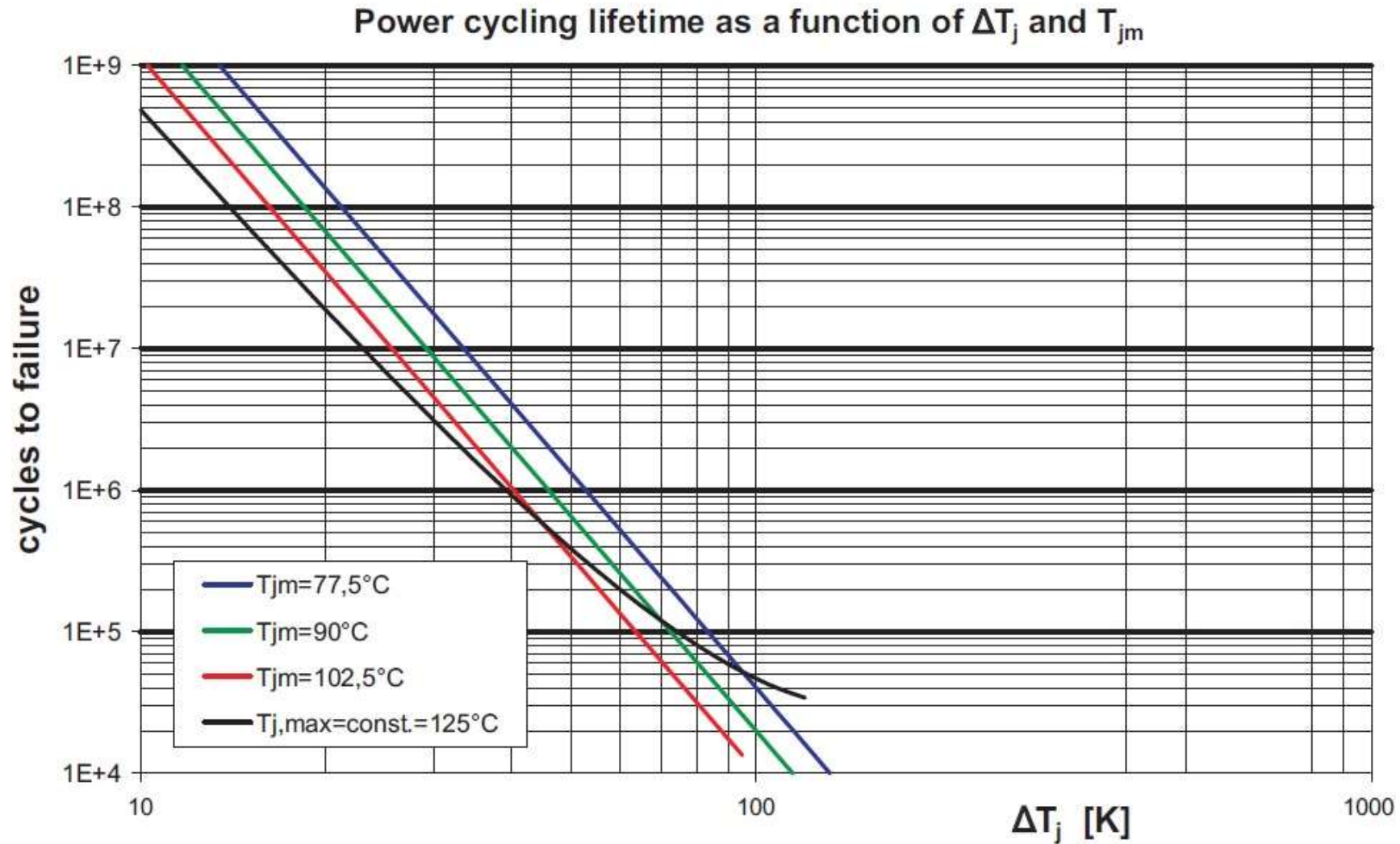
$$I_c = \frac{\sqrt{R_{thJC} \cdot V_{T0}^2 + 4 \cdot RCE \cdot (T_{j(max)} - T_c)}}{2 \cdot \sqrt{R_{thJC} \cdot RCE}} = \frac{V_{T0}}{2 \cdot RCE}$$

## 2. Increase reliability → number of power cycles

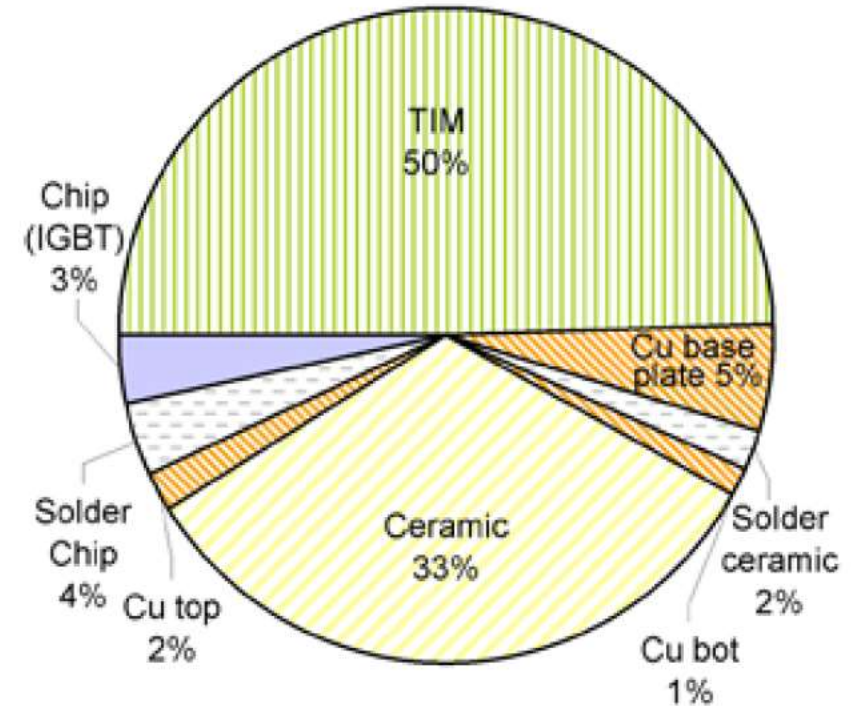
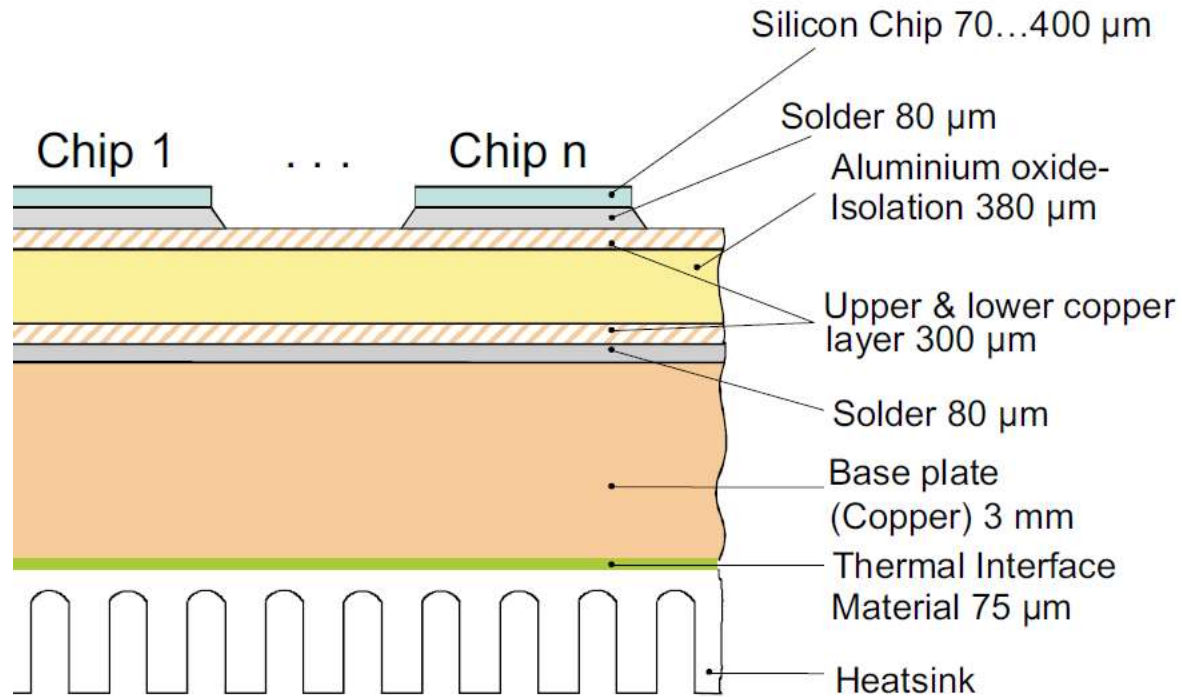
- Number of power cycles will decrease with increasing  $T_{jop}$

## 3. Cost optimization

# Lifetime Industrial Standard

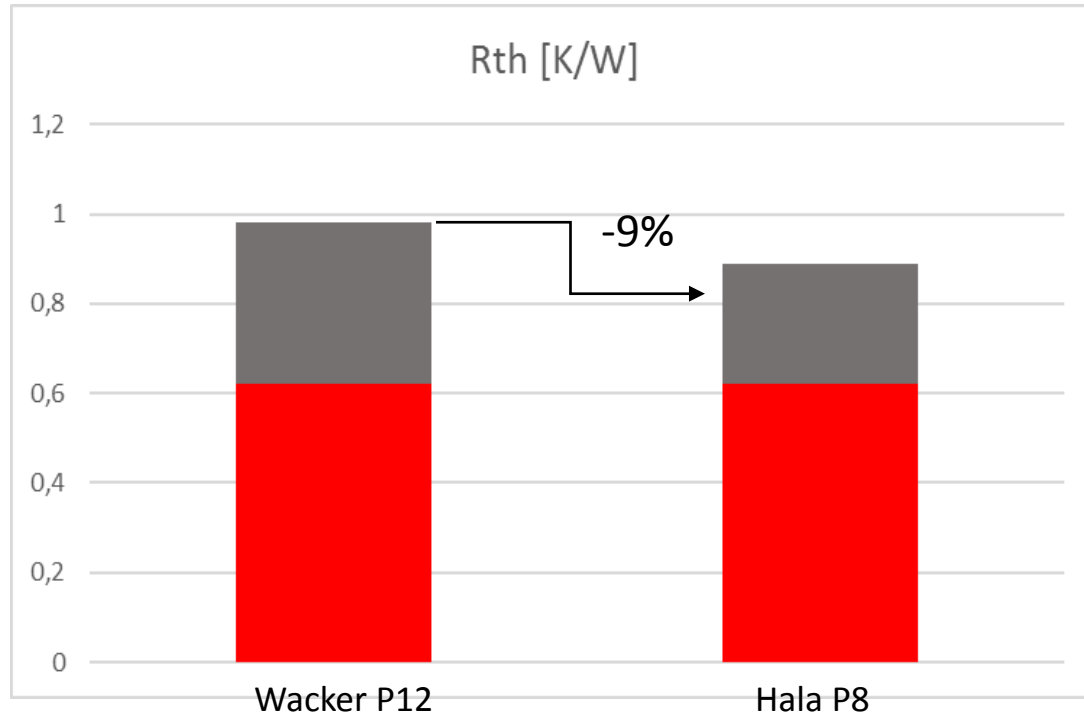


# Thermal losses for standard modules

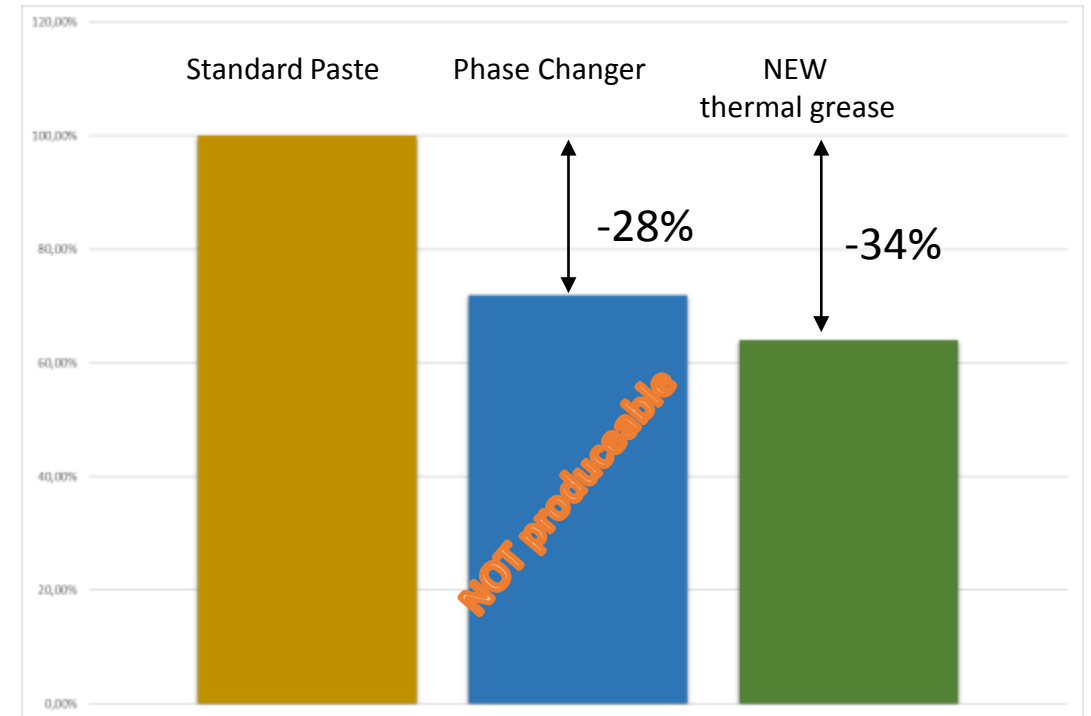


Source: Semikron Application Handbook

# Pre-applied TIM

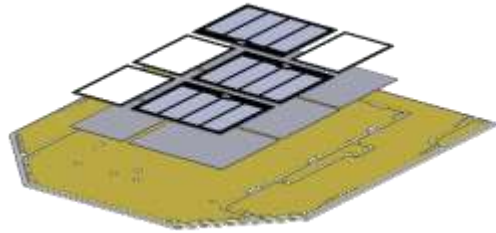


Modules with Baseplate



Modules without Baseplate

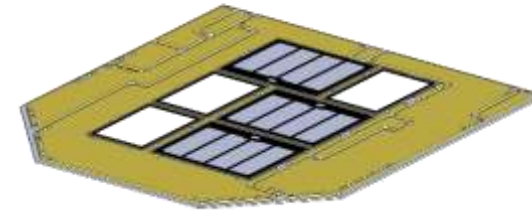
# Sintering instead of Soldering



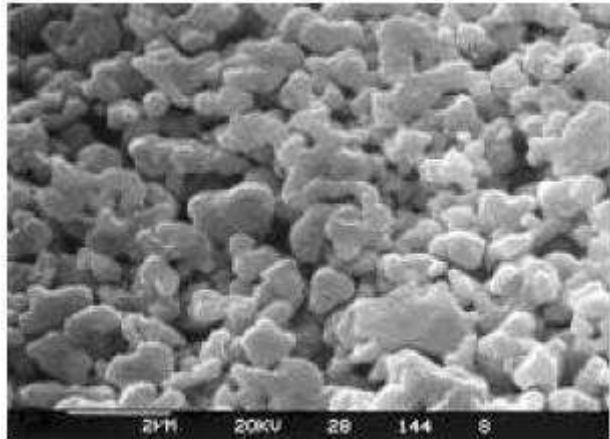
Ag nano particles



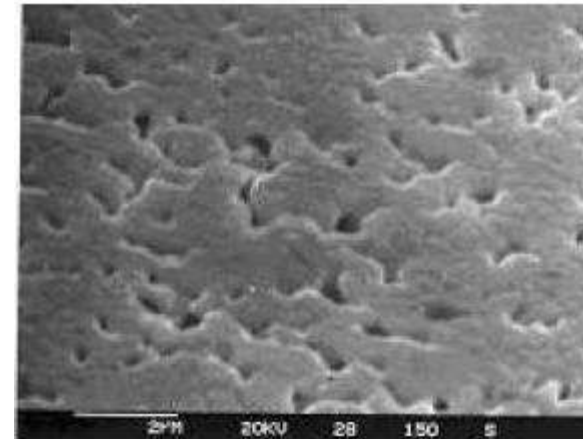
Sintering press



Density of sintered layer very close to density of Ag

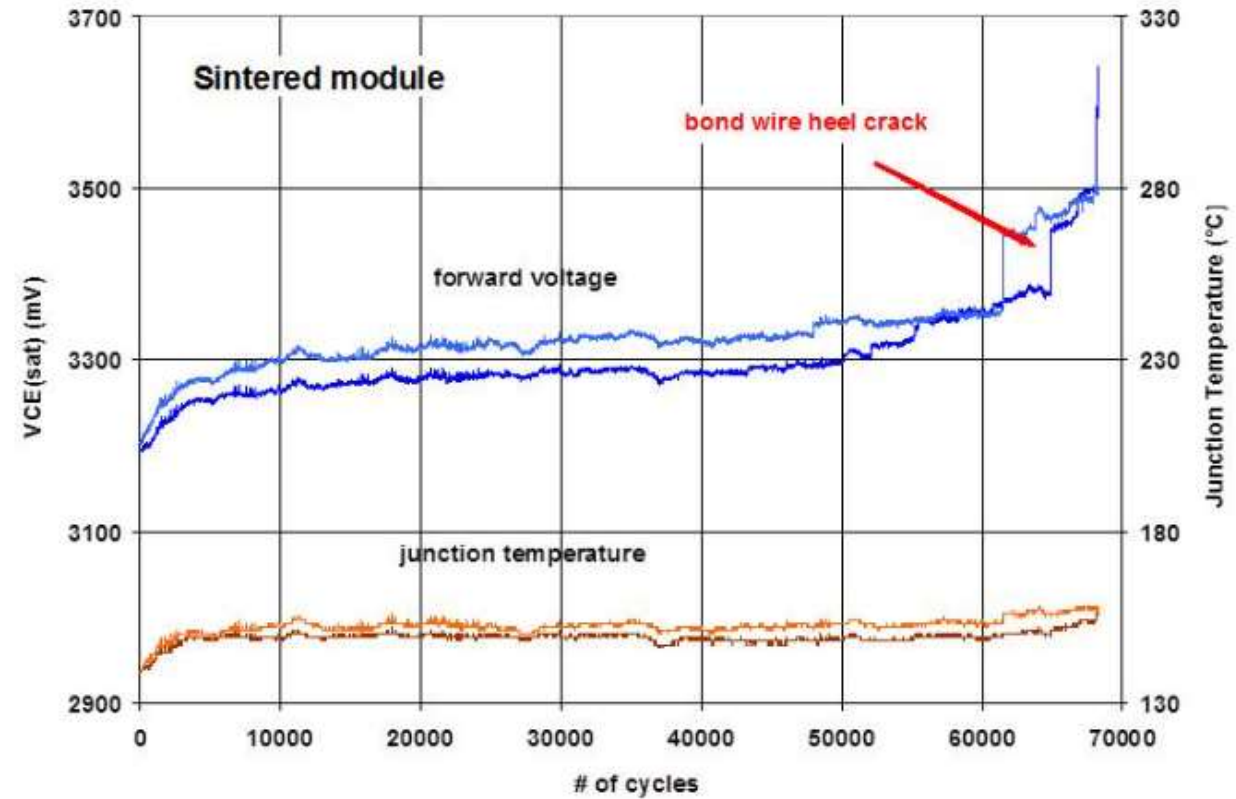
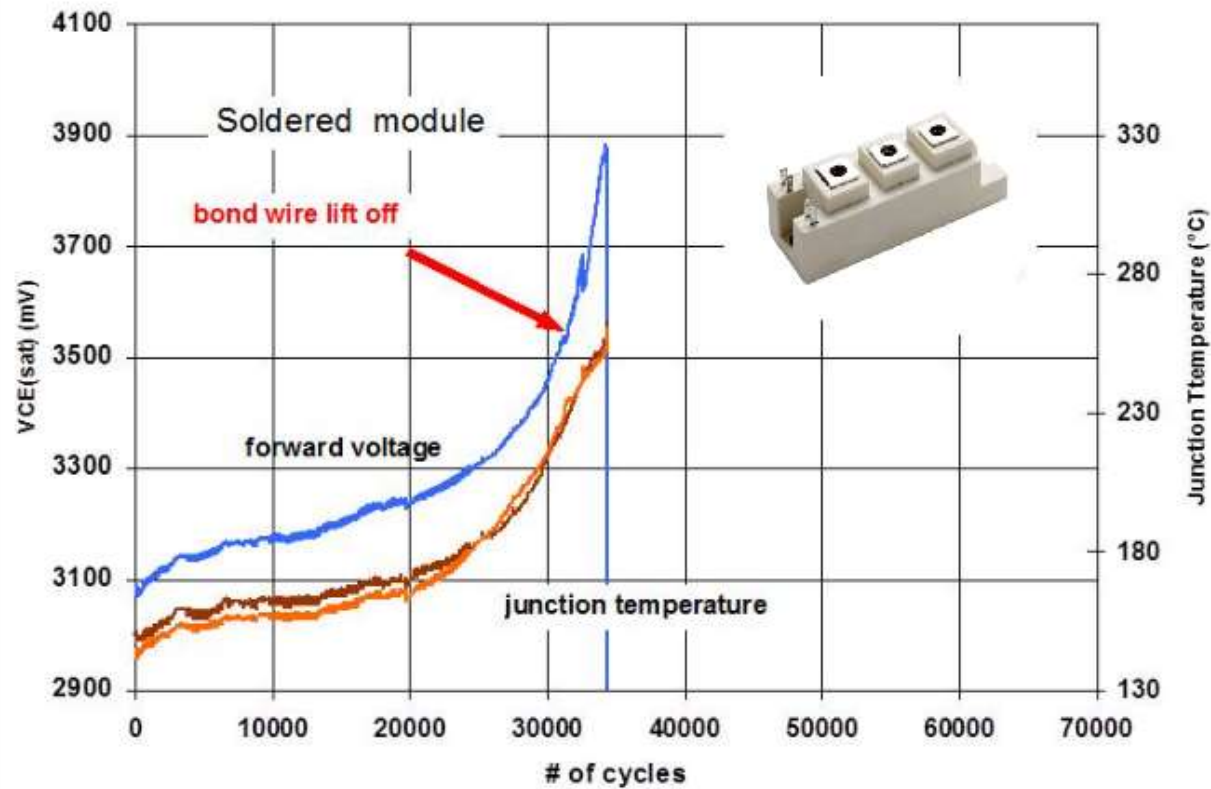


Temperature & Pressure



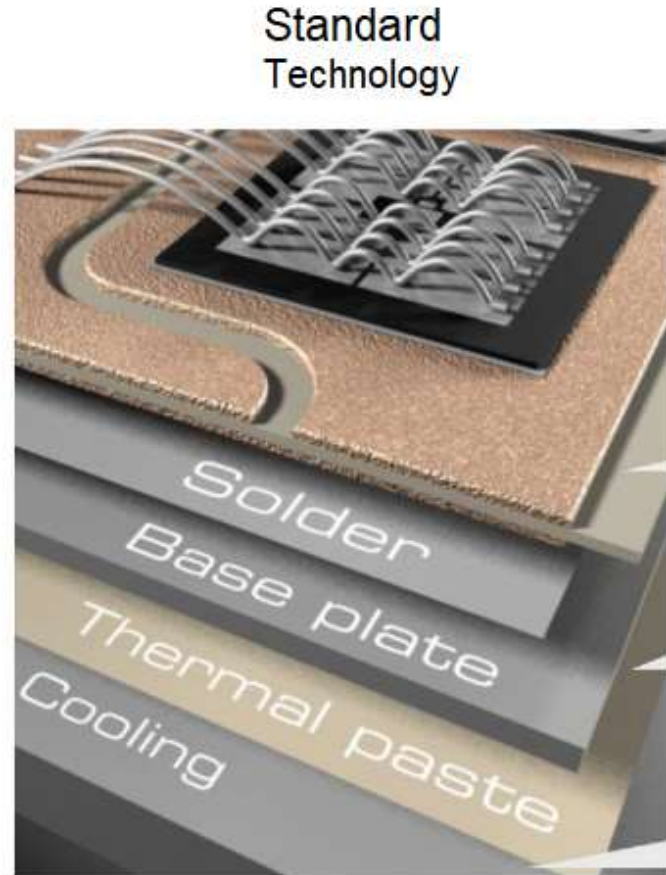
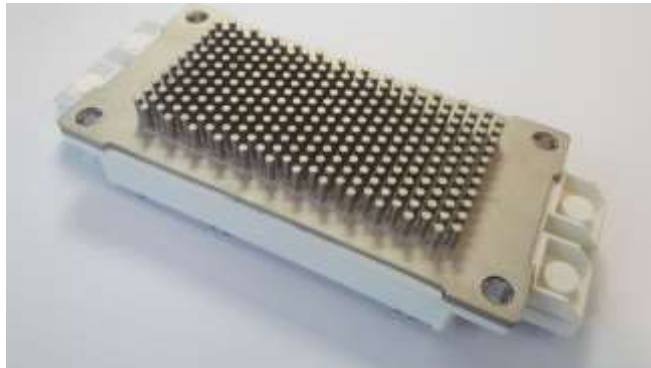
- Fine grained Ag particles sintered at 250°C
- Achieving a very stable connection chip-DBC up to Ag melting point of 962°C
- 4 x increased melting temperature of Ag compared with standard solder results in 3 x higher power cycling capability

# Sintering instead of Soldering

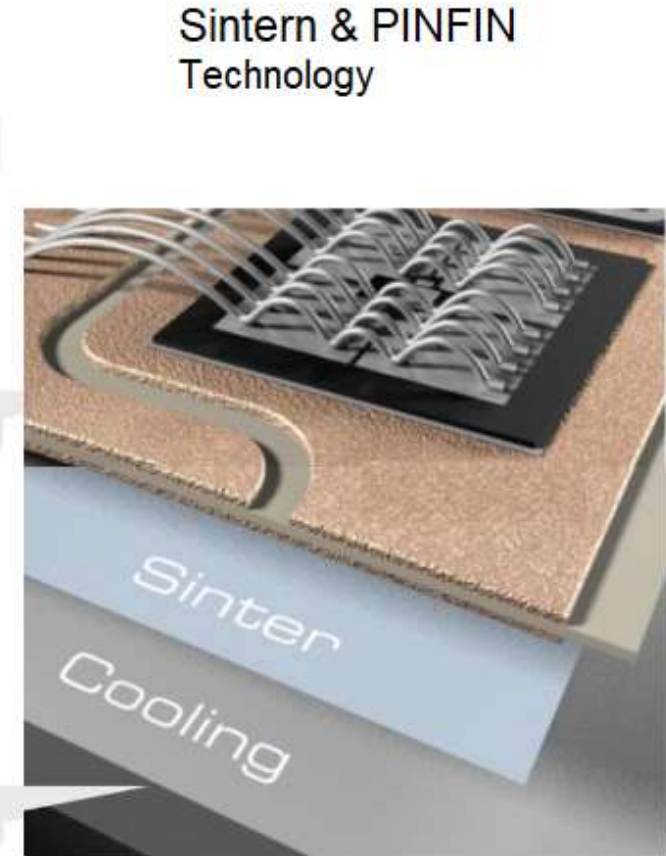


# PINFIN

- Sintering DBC with sintered chips straight to the heatsink will allow a design without baseplate and TIM
- Achievable reduction in  $R_{thj-a}$  of about 25%



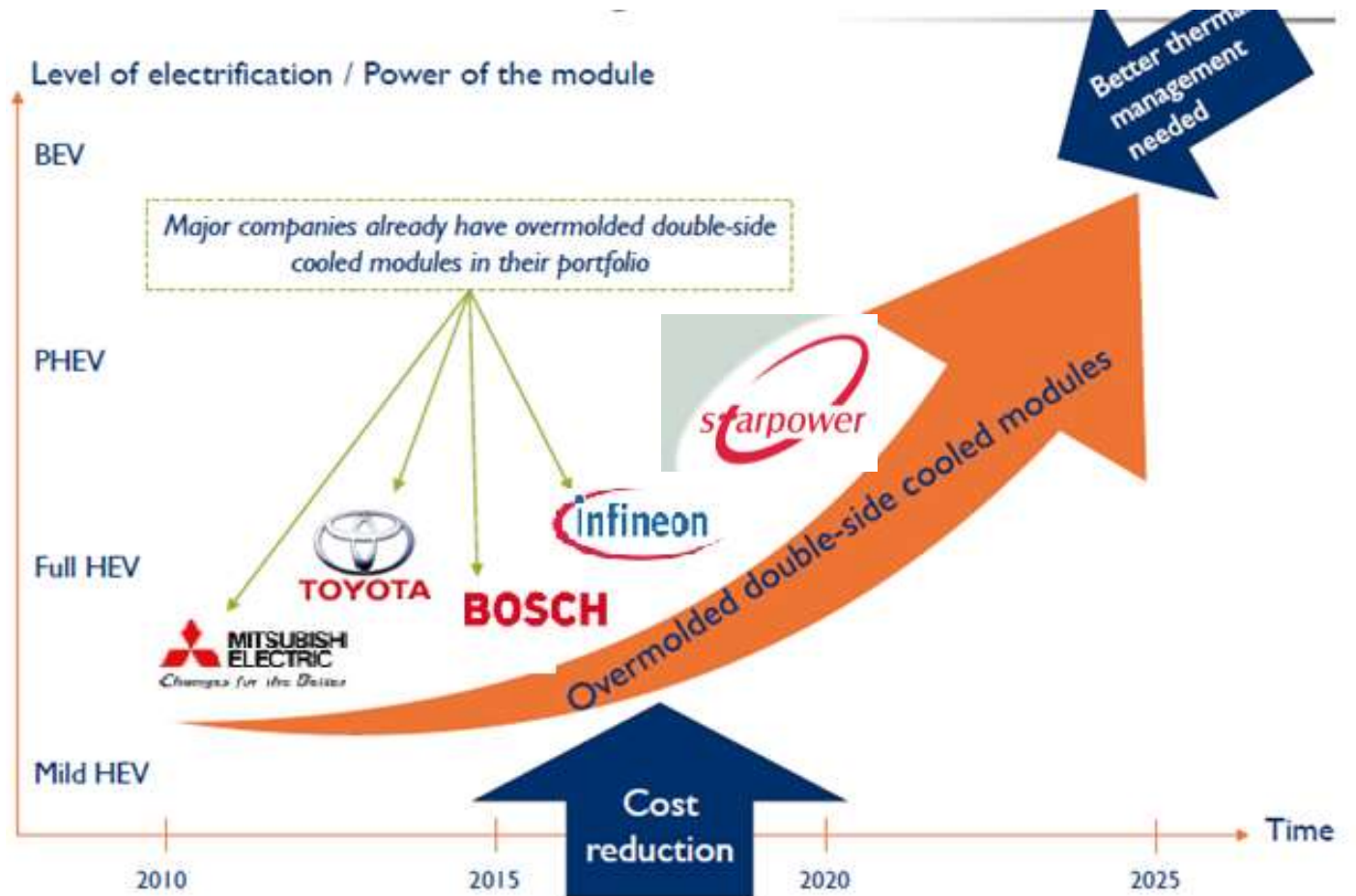
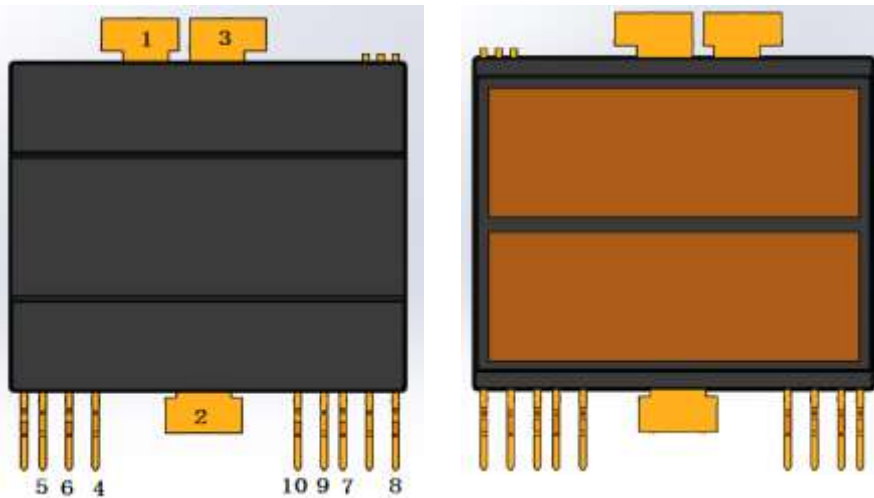
$R_{th[j-a]}$ [K/W]	
0.85	0.61
Chip + DCB	0.25
Thermal paste	0.25
Cooling	0.35



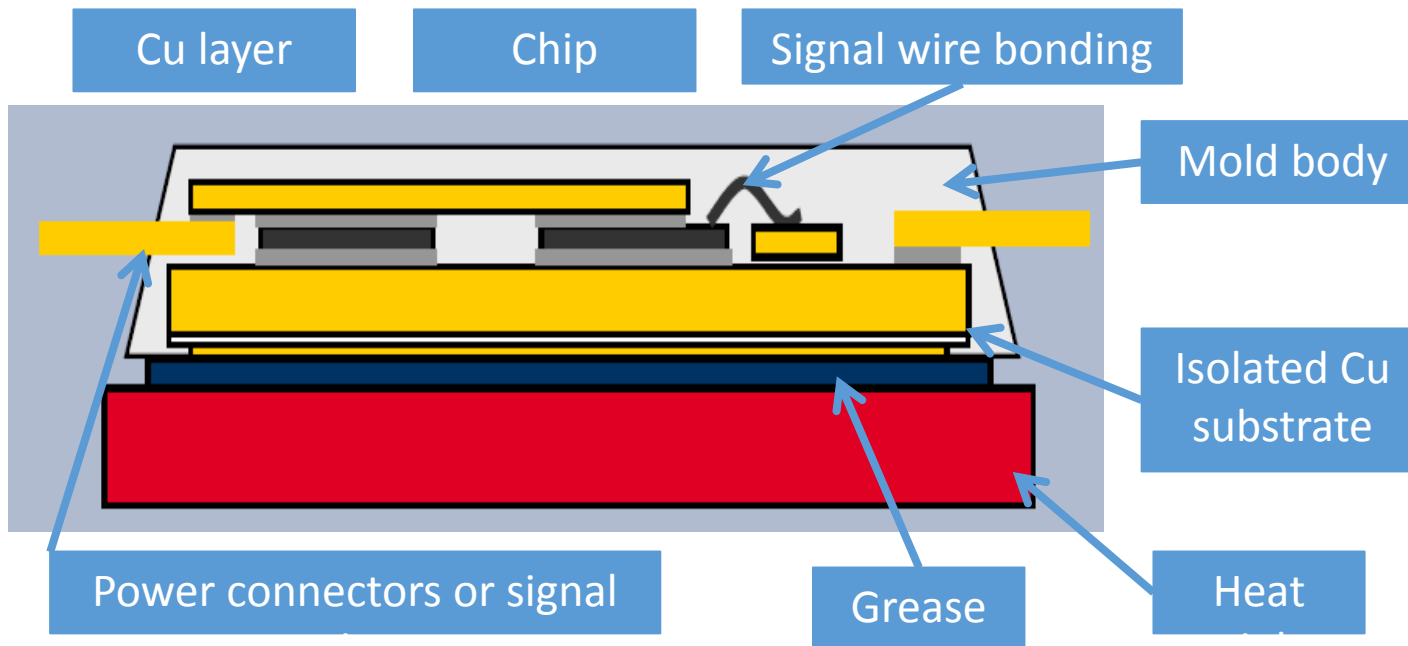


# Single & Double Side Cooled Modules

- Highest power density per module size in order to facilitate space and performance requirements for EV-applications
- Better thermal management due to double side cooling



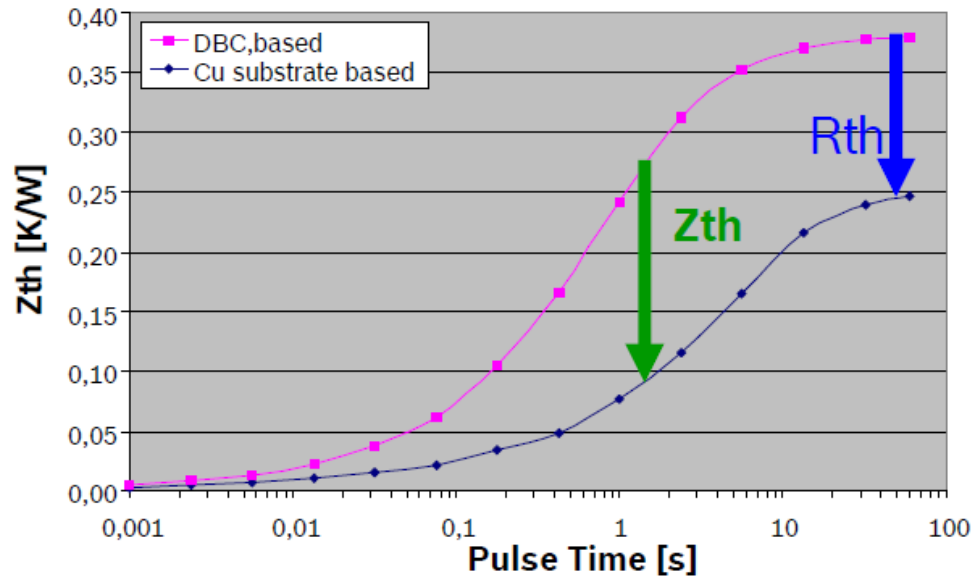
# Single & Double Side Cooled Modules



- Smallest package size / A  
→ Low cost
- Heat can be dissipated in two directions  
→ Efficient heat dissipation  
→ High power density
- Small package height, DC+/- close together, no bond wires  
→ Low parasitic inductance
- Massive copper terminals around the dies  
→ Low losses  
→ Large thermal capability  
→ Low  $T_j$  fluctuation

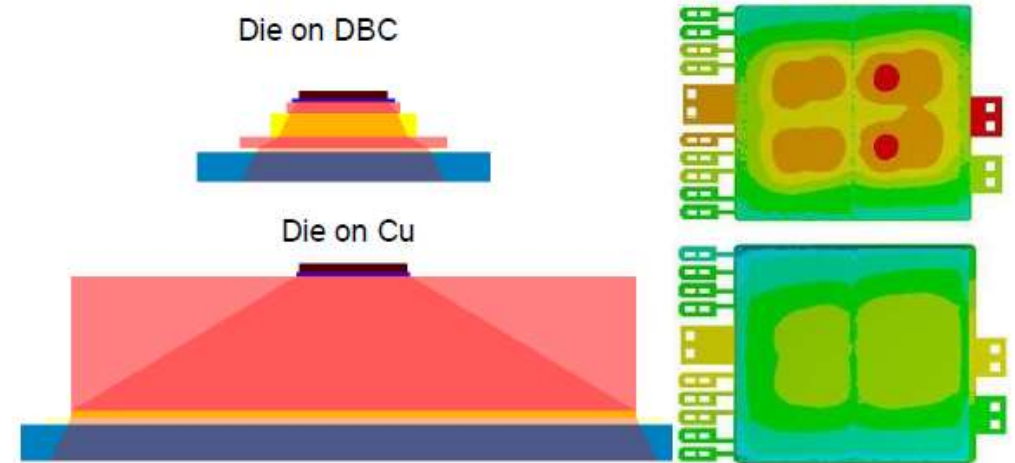
# Core Technologies: Current Density by Design

Comparison DBC vs. isolated Cu substrate



## Reduced power dissipation:

- Low ohmic module design and IGBT-contacting
- Low inductive module design



## Improved heat flow to heat sink:

- Up to 70% improvement in  $Z_{th}$
- Up to 30% improvement in  $R_{th}$

Due to

- double sided IGBT cooling by solder contacting
- optimized heat spreading by thick Cu layer

# Common Packages

