SEED

(System-Efficient ESD Design)

EMCMCC

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Bibliography

Mart Coenen has over 35 years experience in EMC in various fields and has published books and many National and International papers.

He is involved in international EMC standardization since 1988. He was project leader of the standards: IEC 61000-4-6 (Immunity to conducted disturbances induced by radio-frequency fields) and IEC 61000-4-2 (Electrostatic discharge immunity test).
He is past convener of IEC TC47A/WG9 and member of WG2 for which he was given the IEC 1906 award in 2006 after publishing various parts of the IEC 61967-x, IEC 62132-x and IEC 62215-x series.

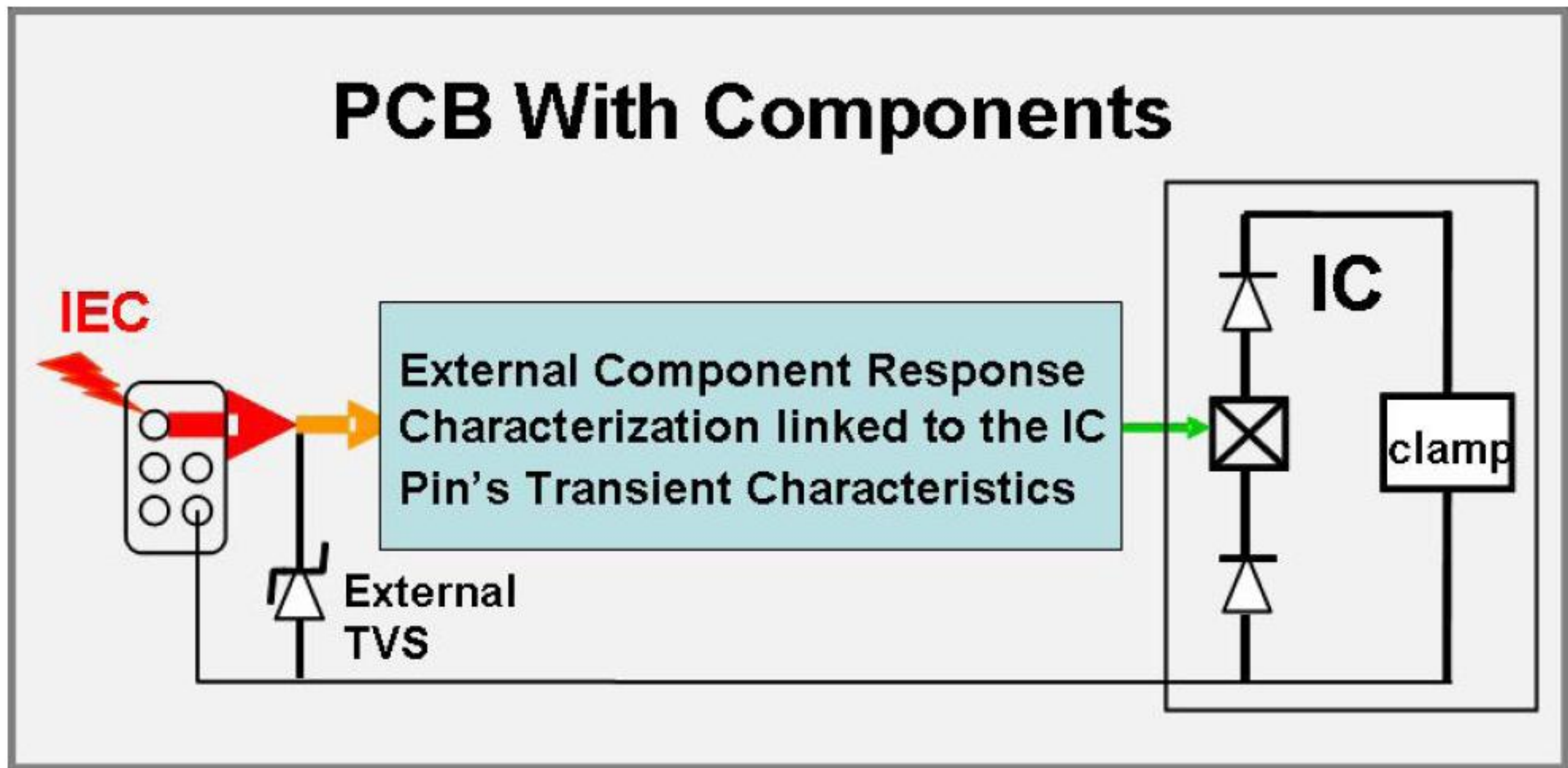
He is co-founder of the Dutch EMC/ESD Society, part-time lecturer at Post Academic EMC courses for the last 27 years and now at Fontys University of Applied Sciences.

Since 1994 he owns his private consulting company EMCMCC, where he focuses on EMC and other system integration issues in e-Hardware

Outline

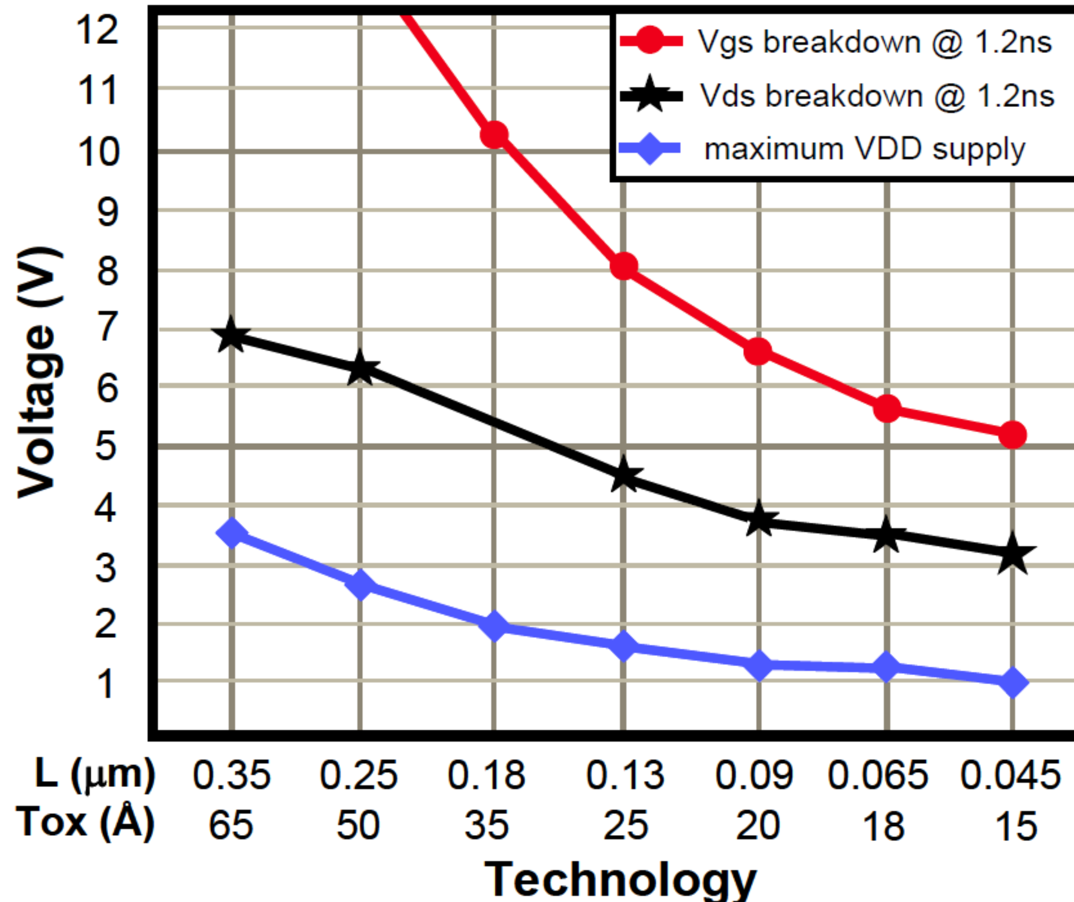
- SEED intro
- TLP testing
- SEED
- Non-linear behavior
- Primary ESD protection
- Conclusions

SEED (System-Efficient ESD Design)



System-Efficient ESD Design concept requires careful consideration of interaction between the PCB protection and the IC pin transient characteristics.

SEED (System-Efficient ESD Design)



Source: White Paper 2: A Case for Lowering Component Level **CDM** ESD Specifications and Requirements, Industry Council on ESD Target Levels

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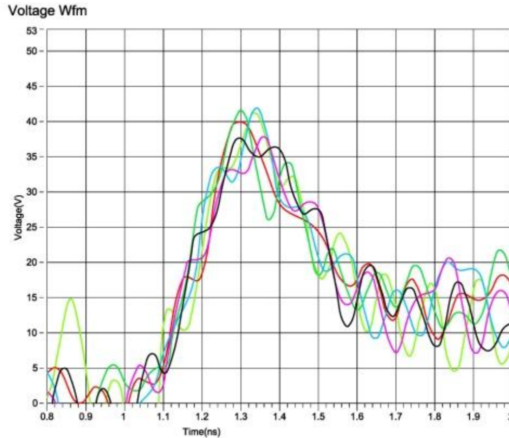
TLP



TL1, $Z_o = 50\Omega$

TL

Current Probe

500Ω

56Ω

DUT

High Voltage Supply

Termination

$V_{DUT}(t)$ $I_{DUT}(t)$

TLP

White: voltage, Red: current

TLP

Too many variables with TLP testing:

- Impedance; 50, 500 Ω
- Duration; 1 ns – 1 μs
- Attenuation dependent multiple reflections
- Risetime; <100 ps to several ns
- Waveshape; regtangular or IEC (HMM)

Most TLP testers responses are measured falsely or incomplete!
Single point at 70% of the pulse width with too low bandwidth

TLP Device testing

- Testing-wise only TLP test method is suited to be used with a coaxial switch matrix (50 Ω) towards multiple IC pins to be tested
- Most TLP generators are non-optimal build and suffer from severe reflections (= non-issue @ 70% of pulse)
- TLP testing is artificial compared to the real-life ESD phenomena occurring but …
  - TLP testing is very reproducible but often wrong applied
  - TLP is fast …
  - (vf)TLP is very fast … but shorter

SEED (System-Efficient ESD Design)

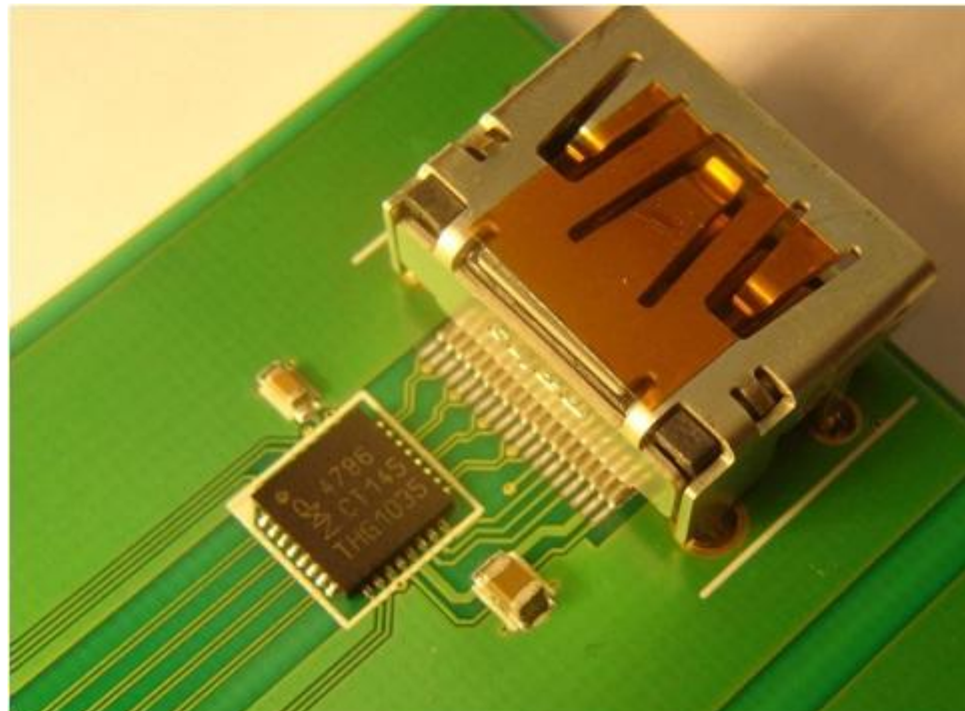
- **Primary** ESD protection
  - What, where, how, to what reference, when should it trigger, how should it respond (clamp) ?
- **Secondary** ESD protection
  - What, where, how, to what reference, when should it trigger, how should it respond (clamp) ?
    Typically at the boundary of the IC to protect the inner circuits
- To protect what ?
  - RF, Digital I/O, processor core, etc.

SEED (System-Efficient ESD Design)

Which device reacts first ??

- Well-balanced signals
- Ground pad underneath package to PCB
- X-coupled over device

- Too long distance to voltage clamping reference



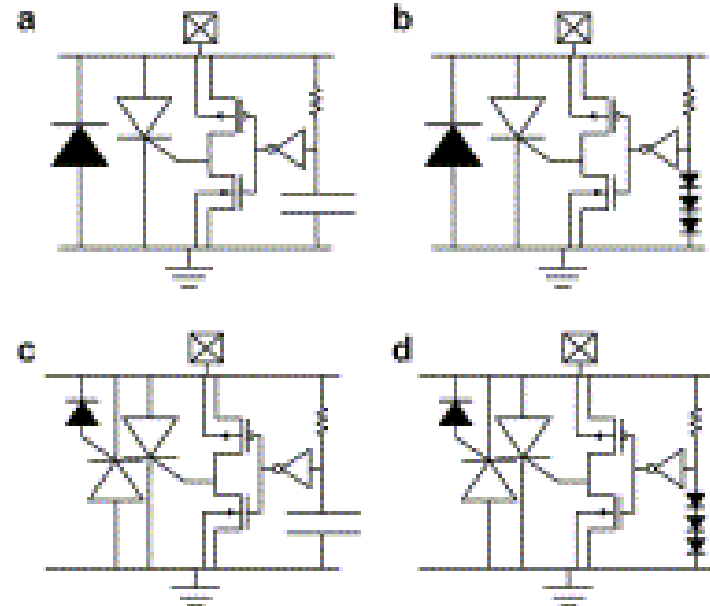
HDMI ESD protection example with external references

SEED (System-Efficient ESD Design)

- Primary ESD protection determined by functional signal amplitude and bandwidth:
  - Mobile phone: 2 Watt in 50 Ω → 10 Volt RMS @ 900, 1900 MHz
  - HDMI/ USB3/ FireWire: several Gb/s
- Protection determined by other functional/EMC requirements
  - Automotive (CAN/LIN): 5 Watt (37 dBm) in 50 Ω
→ 32 Volt peak EMF @ 0,1 -1000 MHz
- Protection needed in-between 'floating' voltage domains/ IC blocks: I/O, core, analogue, oscillator, etc.

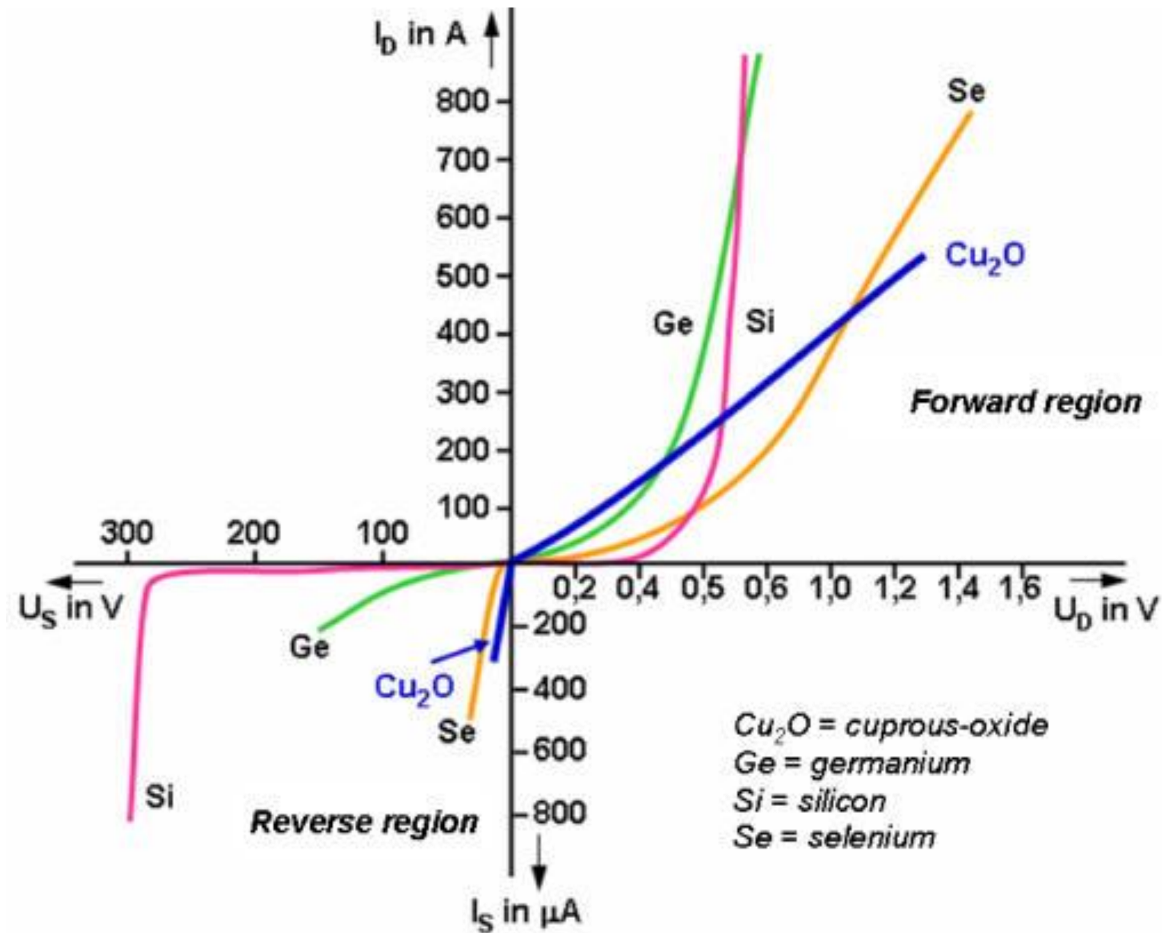
Non-linear behavior

- **ESD Protection devices (biased/non-biased):**
  - Diodes (anti-parallel)
  - ggNMOS
  - BigFets (many patents)
  - Zener diodes
  - TVS
  - SCR
  - VDR

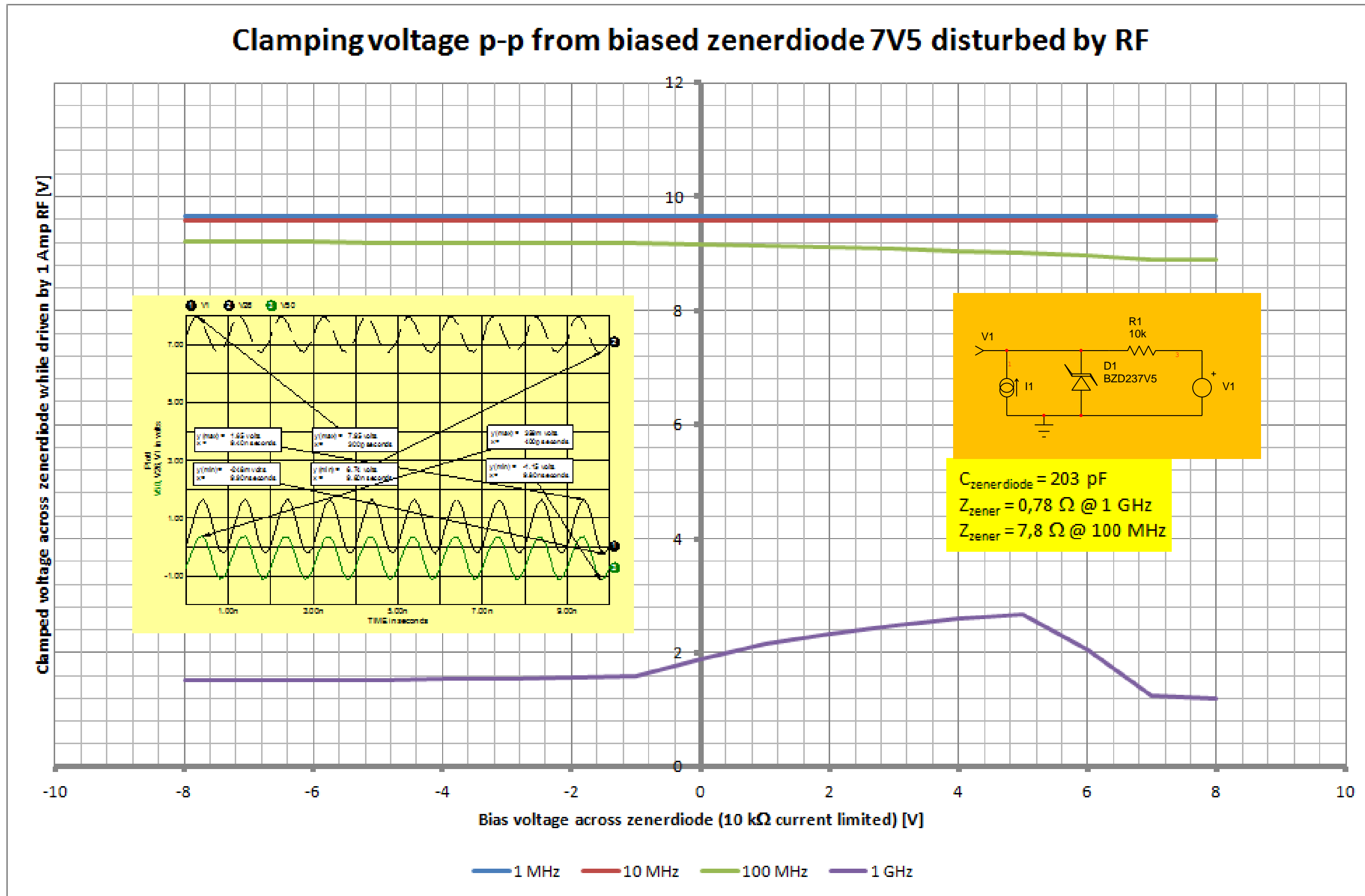


a) SCR + dynamic triggering,
b) SCR + static triggering,
c) bi-SCR + dynamic triggering,
d) bi-SCR + static triggering.

Non-linear behavior

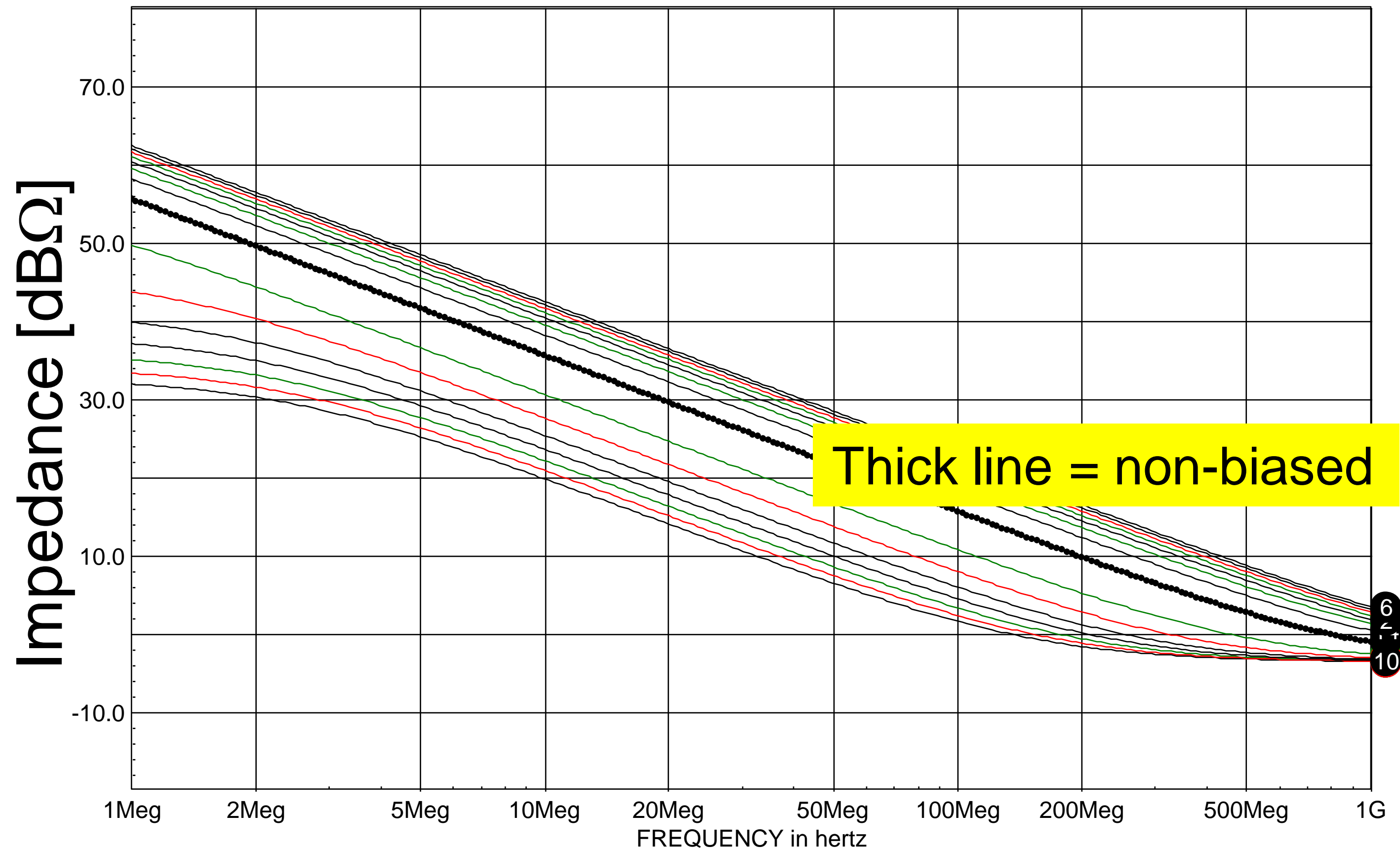


Non-linear behavior vs frequency



Non-linear behavior vs frequency

zenerdiode



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Non-linear behavior vs frequency

TVS

Impedance [dBΩ]

80.0
60.0
40.0
20.0
0

1Meg 2Meg 5Meg 10Meg 20Meg 50Meg 100Meg 200Meg 500Meg 1G

FREQUENCY in hertz

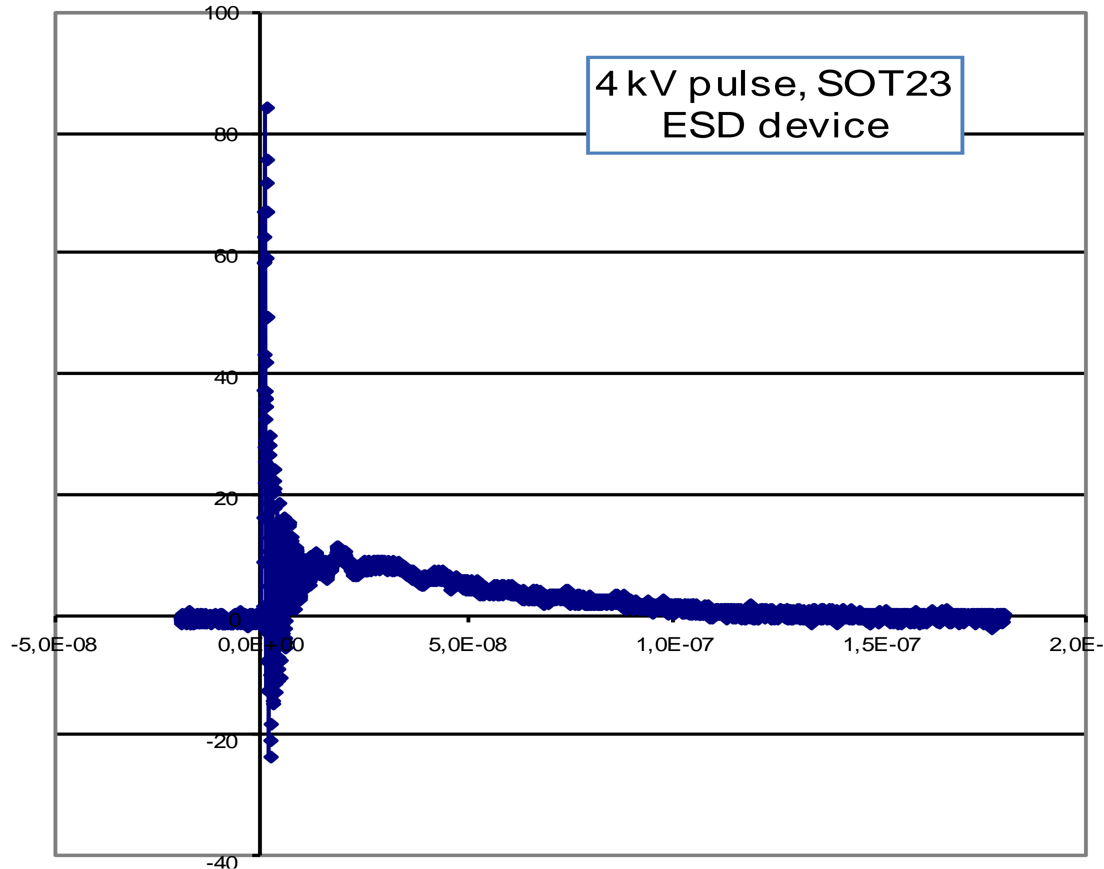
Non-linear behavior

- Non-linearities may occur outside the functional but within the (over-)stress voltage level ranges
- With the on-chip ESD protection devices a high-pass filter is typically used for the ESD protection triggering circuit
  - Clamping shall be fast but short
  - If dV/dt isn't met, the device doesn't trigger !

Where, what ?

- ESD overvoltage/current needs to be limited without insulation breakdown and/or thermal damage
- ESD protection needs to be fast: typ. ≤ 1 ns
- ESD clamping voltage needs to be set just above working voltage or EMC stress level
- Current paths need to be as far away as possible from ESD sensitive pins
- Primary ESD protection: as close as possible to connector ?

Primary ESD protection



Primary ESD protection

The off-chip protection has to:

- Reduced the ESD energy by orders of magnitude (before it gets to the device)
- Has to able to handle the energy and power
- Have a rate of rise which is the same or faster
- Have a minimum voltage peak occuring prior to voltage clamping due to path inductivity and avalance effects

Primary ESD protection

Off-chip protection has to:

- Be faster than the on-chip one
- Clamp earlier
- Capable of handling more energy/current

Furthermore:

- It has to be small
- Leadless i.e. minimal series inductance
- It may not add capacitance to the signal lines
- Has to remain transparent/ linear until clipping

Primary ESD protection

According IEC 61000-4-2, discharge:

- To metal connector shell only (in most cases)
- Only to pins when connector (shell) in non-conductive
- Charged (shielded) cable is ignored
- Excluded on connectors with ESD warning
- Rep.rate is just indicative: e.g. 1 pulse/s or the time necessary to recover

Connectors are being designed to have shell contact before they have pin contact (CDE)

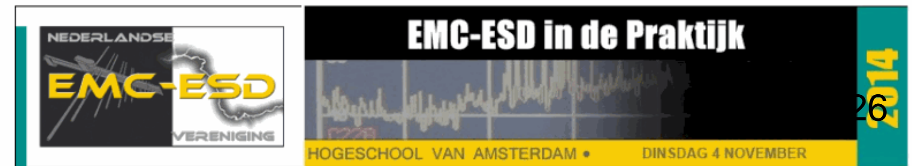
Conclusions

- Nanometer devices are becoming much more sensitive to ESD:
  - E-field across thinner insulation barrier
  - Thin and narrow metal w.r.t. thermal heating
- On-chip ESD protections need to be faster
  @ less clamping voltage and earlier triggering
- Complementary off-chip protection measures
- New ESD testing methods required

Conclusions

- Most 'conflicts' between ESD and functional application requirements are typically self-initiated by:
  - Poor chosen on- and/or off-chip ESD protection circuits
  - Non-utilized measures in-package or on-chip by non-optimal application/design architecture
  - With appropriate off-chip clamping and filtering measures, the ESD energy (to cope with on-chip) can be reduced (as the IC can't handle it all !!)
  - Cascadable ESD test methods are needed which can handle complimentary ESD protection measures

Q&A



Acknowledgments

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  - Sandeep Bakshi with whom I've developed the SII test method (now IEC 62215-2)
  - Many of my automotive customers, who suffered RF immunity issues due to the ESD protections required