A micrograph of a programmable photonic chip, showing a complex array of waveguides and optical components. The chip is rectangular and features a central area with a grid of waveguides and several larger, more complex structures. The background is dark, and the chip is illuminated, highlighting its intricate design.

Programmable photonics

Leimeng Zhuang
Photonics, imec USA

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Imec world map



BELGIUM - HQ
LEUVEN



THE NETHERLANDS
EINDHOVEN



JAPAN
OSAKA

JAPAN
TOKYO



CHINA
SHANGHAI

TAIWAN
HSINCHU



INDIA
BANGALORE

USA
SAN FRANCISCO



USA
ORLANDO



Imec USA

Opened in 2016

500 acre technology district part of Osceola County's **NeoCity** initiative located in Kissimmee, Florida

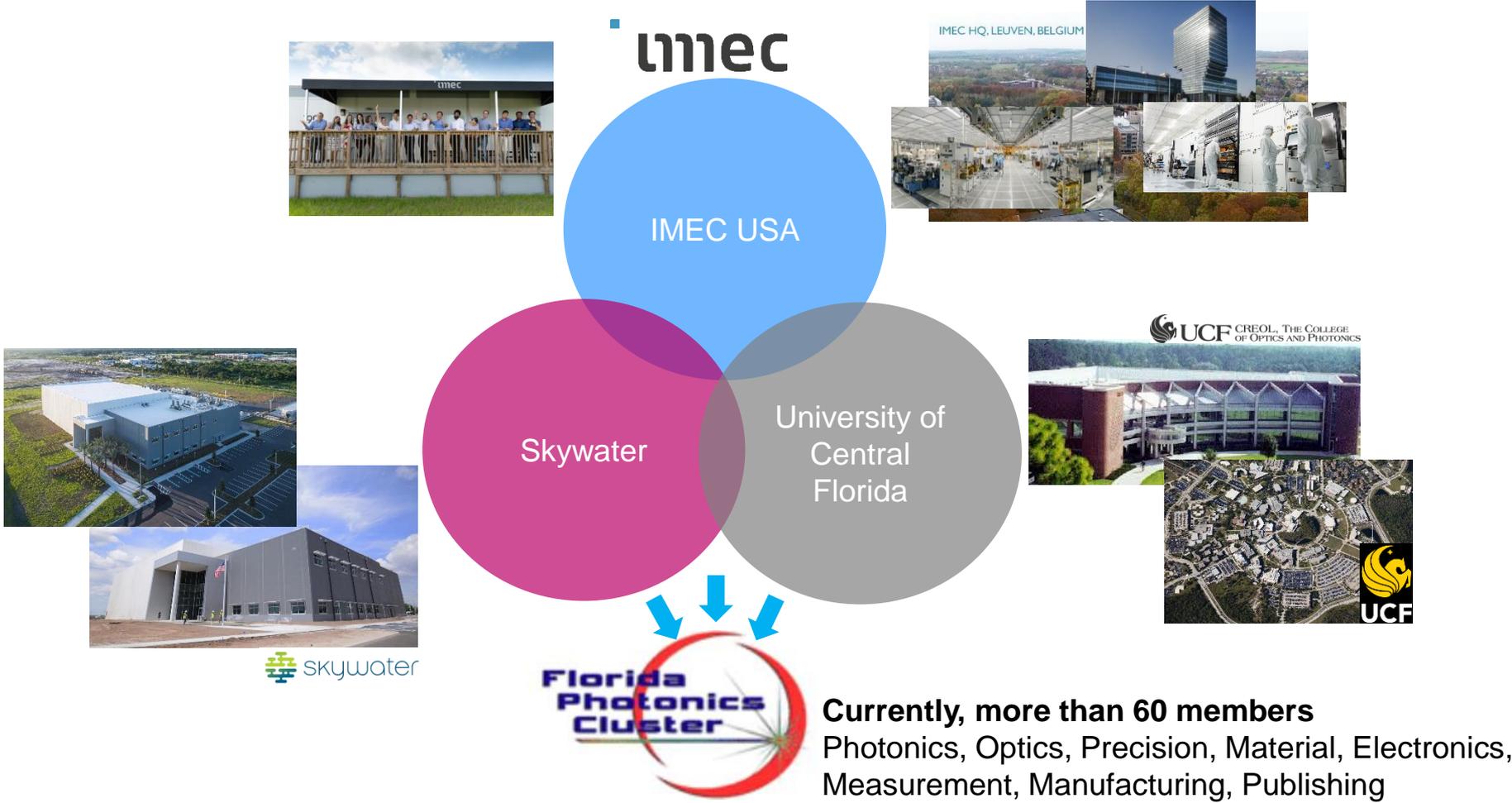
Partnered with **Skywater** for fabrication

Pursuing R&D in

- *Silicon photonics
- *Highspeed RF electronics
- *Healthcare in space



Local photonics eco system



Technical content

1. imec silicon photonics platform

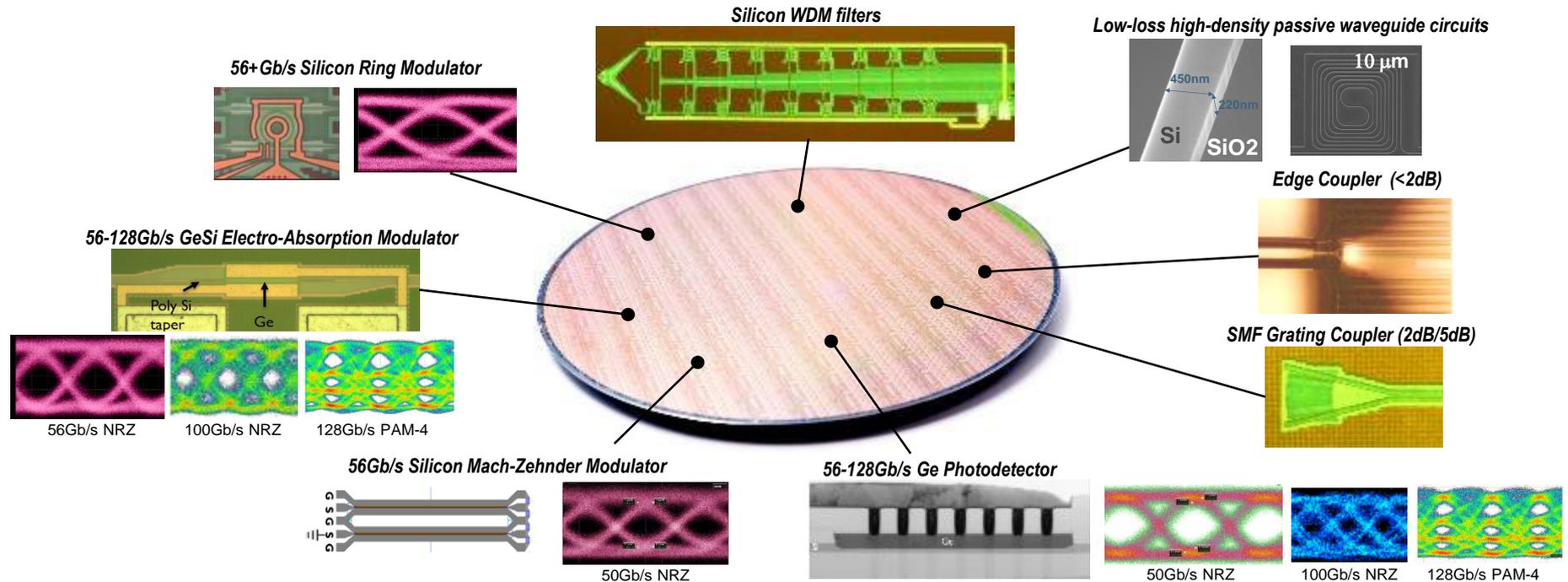
2. Electro-photonics

3. Programmable photonics

IMEC SILICON PHOTONICS PLATFORM

Silicon Photonics Technology Platform

INTEGRATED ON A SINGLE 200MM OR 300MM WAFER

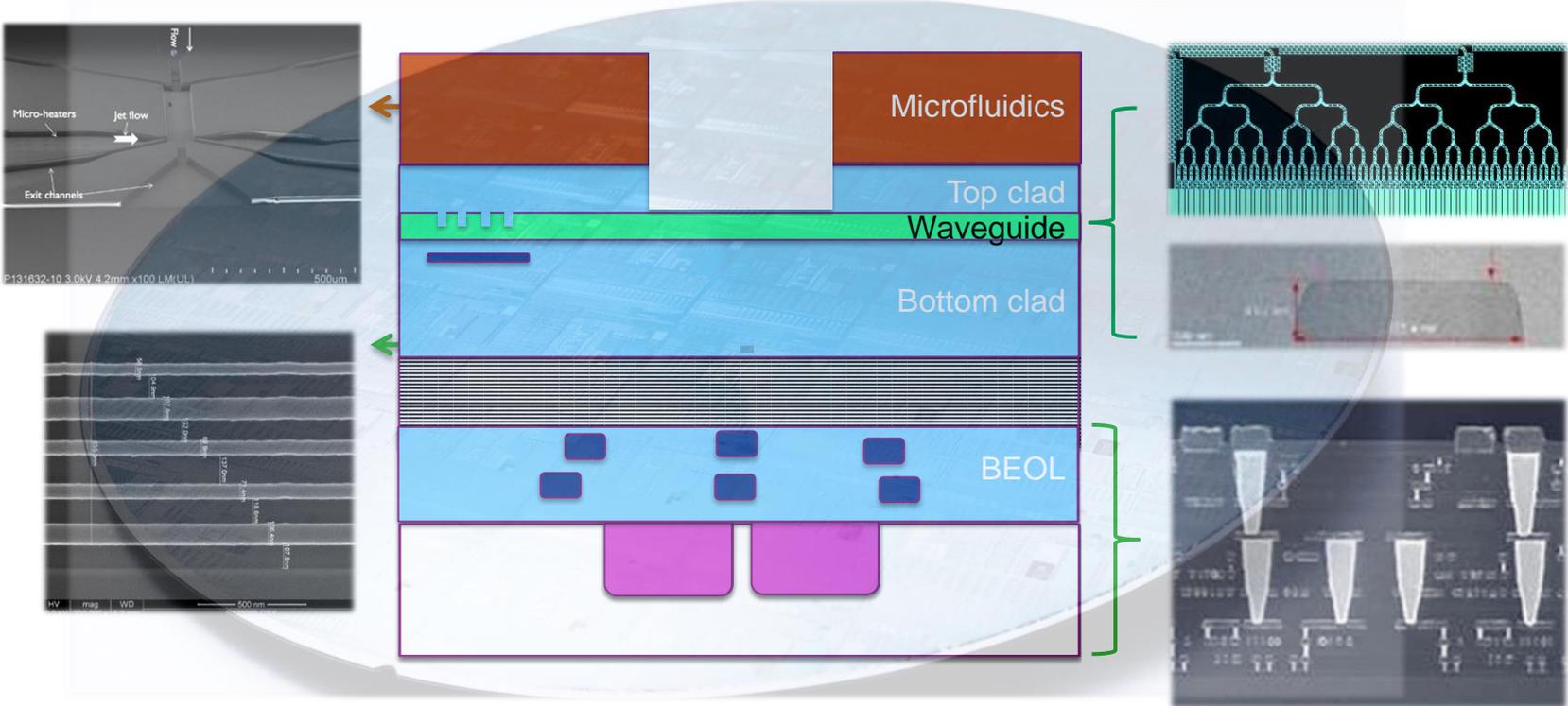


Fully Integrated Silicon Photonics Platform for 1310nm/1550nm Wavelengths

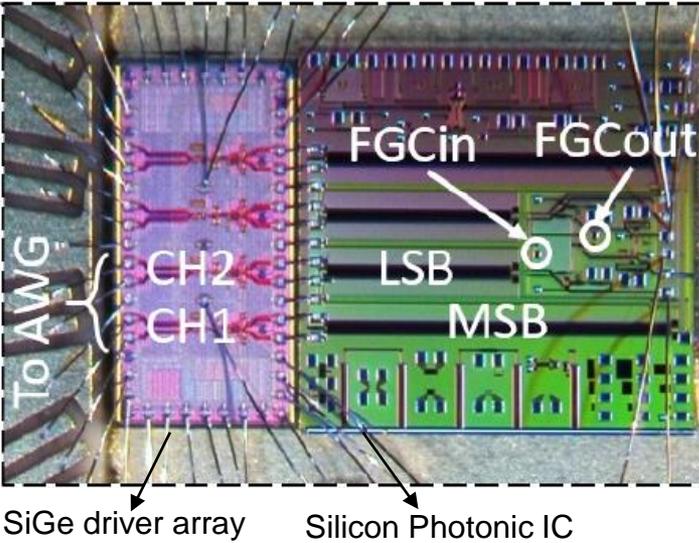
- Low-loss Passive Silicon Waveguide Devices and Fiber Coupling Structures
- 56-128Gb/s (Ge)Si Modulators and Ge(Si) Photodetectors

Integration technology

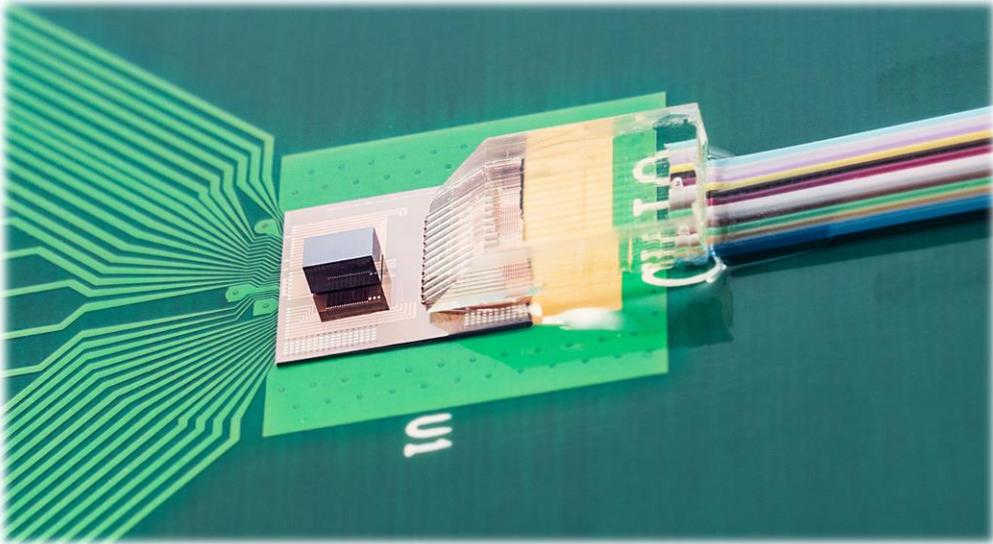
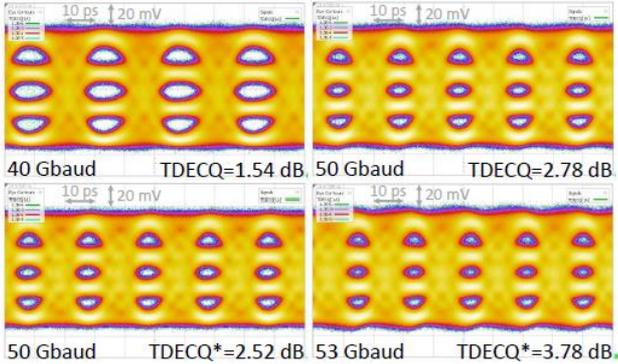
- Versatile, scalable, mature platforms accessing new materials



Packaging



- 55nm SiGe BiCMOS technology
- Silicon Photonic modulator



**TSV-enabled Hybrid FinFET CMOS – Silicon Photonics Technology
for High Density Optical I/O**

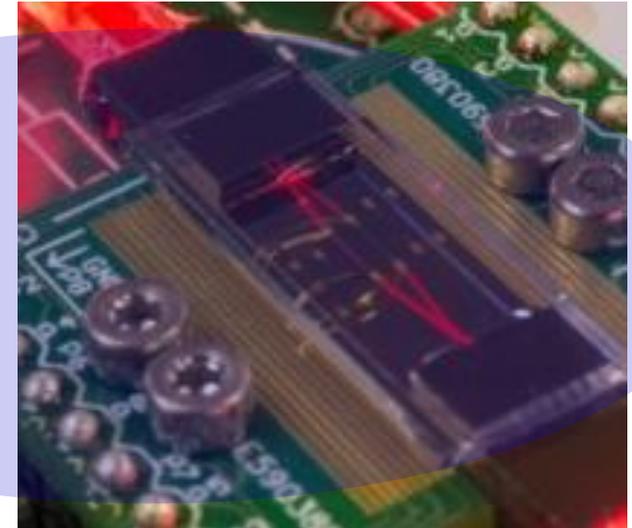
Electro-photonics

Electro-Photonics

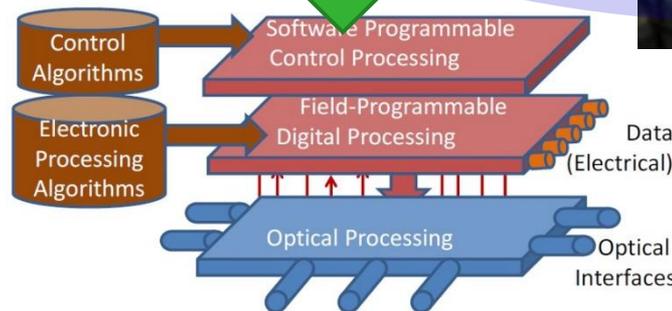
Consider the best mix of **electrical** and **optical** technologies



Electro-Photonics



- Mature industry
- High flexibility
- Easy access to memory



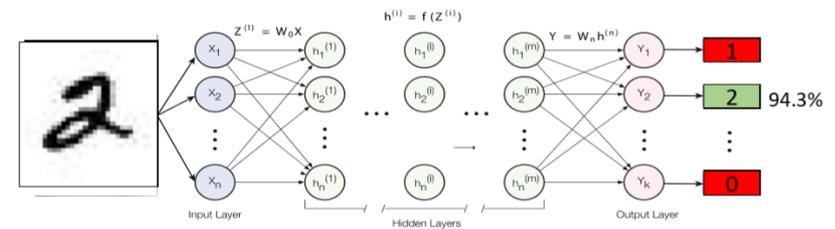
- Large bandwidth
- Energy efficient
- Strong potential for innovation

Prof. Arthur Lowery's ARC Laureate Fellowship, "The Electro-Photonic Interchange: A new green platform for communications signal processing" (2013–2018).

The 1st photonic AI computer

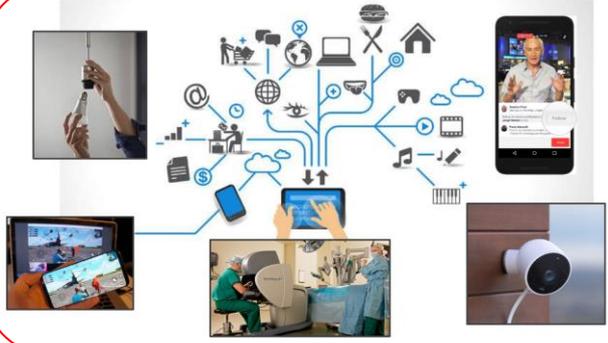


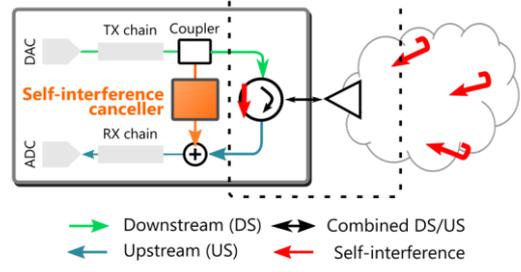
- Self-contained system
- Does not rely on lab environment
- Runs MNIST image recognition
- Better than 97% accuracy



	Electronic Chip	Lightelligence Optical Chip	Improvement
Latency	100 ns	1 – 10 ps	10,000X to 100,000X
Energy Efficiency	1 TOPs/W	> 100 TOPs/W	> 100X
Through-put	30 – 100 fps	> 10,000 fps	> 100X

RF Self-interference cancellation





→ Downstream (DS) ← Upstream (US)
↪ Combined DS/US ↪ Self-interference

GenXComm 

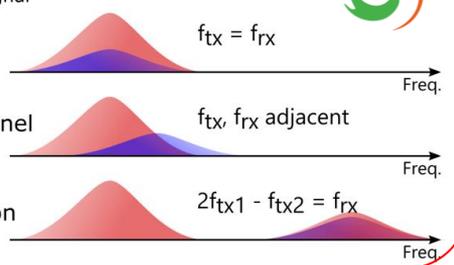
Self-interference

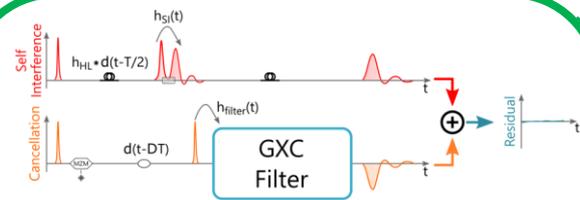
- █ Transmit signal
- █ Receive signal

Co-channel: $f_{tx} = f_{rx}$

Adjacent channel: f_{tx}, f_{rx} adjacent

Passive intermodulation (PIM): $2f_{tx1} - f_{tx2} = f_{rx}$



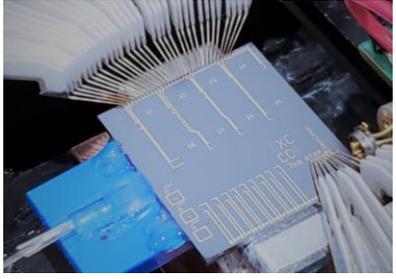


Self Interference: $h_{HI} * d(t-T/2)$

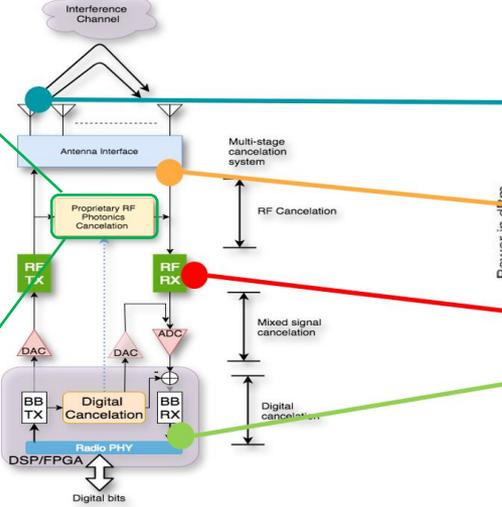
Cancellation: $d(t-DT)$

GXC Filter: $h_{filter}(t)$

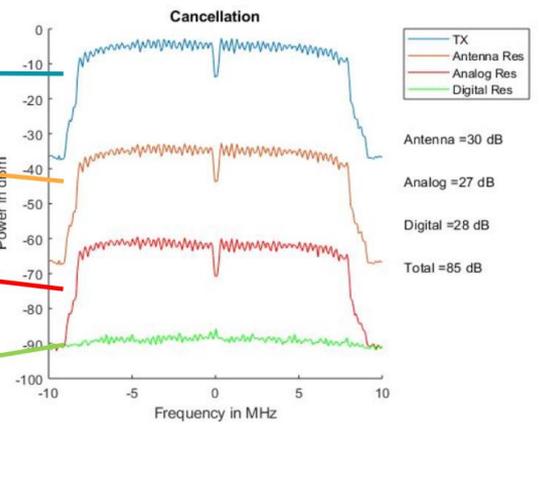
Residual



GenXComm 



Cancellation



Power in dBm

Frequency in MHz

- TX
- Antenna Res
- Analog Res
- Digital Res

Antenna = 30 dB

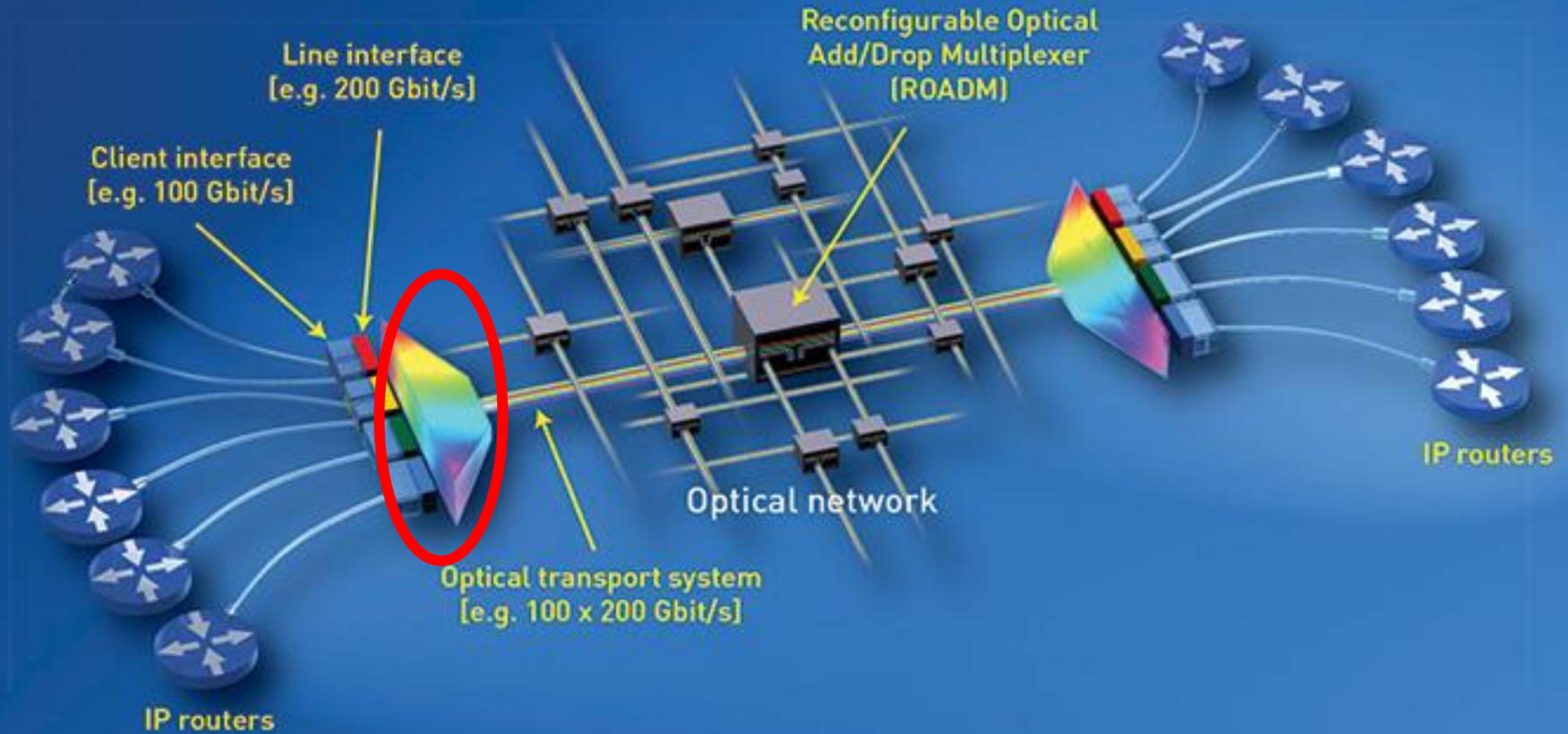
Analog = 27 dB

Digital = 28 dB

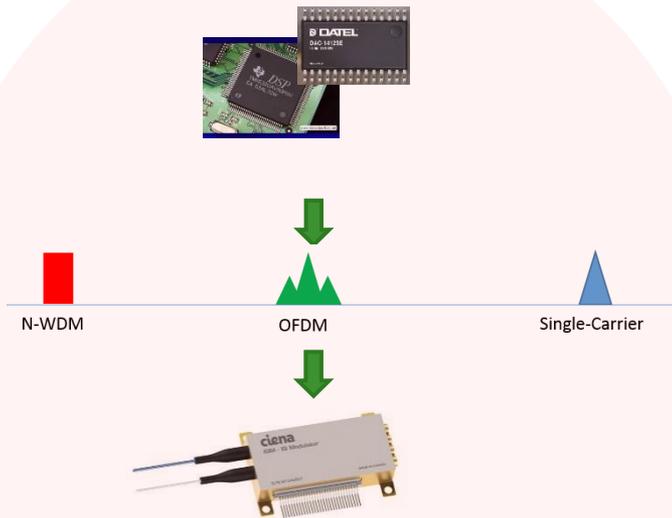
Total = 85 dB

High-spectral-efficiency Tx/Rx

Key components of an optical transport network



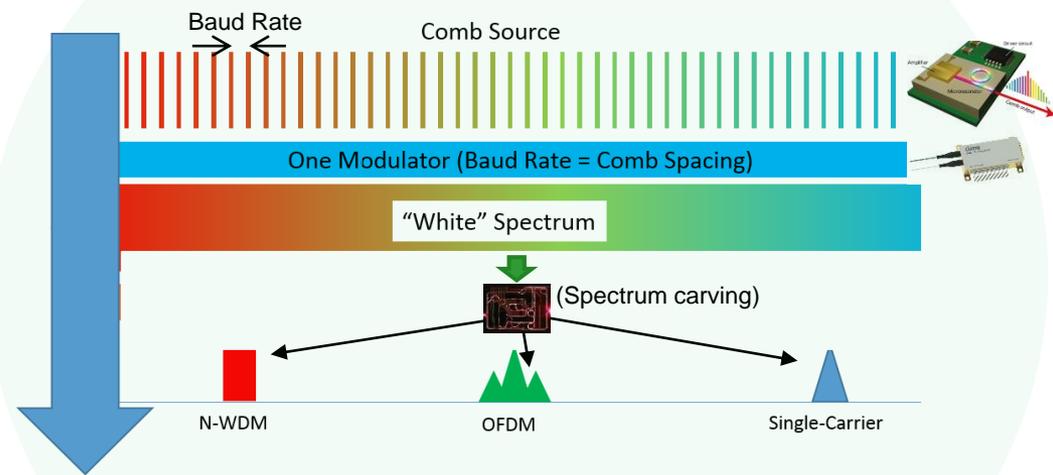
Optical pulse shaping



Electrical shaping (e.g. 25 Gbd/s)

- Fast DSP
- Fast DAC (50GSa/s)
- Fast Modulator

1. K. Lee, C. T. D. Thai, and J.-K. K. Rhee, Opt. Express **16**(6), 4023–4028 (2008)
2. Y.-K. Huang, D. Qian, R. E. Saperstein, P. N. Ji, N. Cvijetic, L. Xu, and T. Wang, OFC 2009, paper, OTuM4.
3. A. J. Lowery & L. B. Du, Opt. Exp., **19**, 15696-15704 (2011)
4. J. Schröder, et al., J. Lightwave Technol., **32**, (2014) pp. 752-759

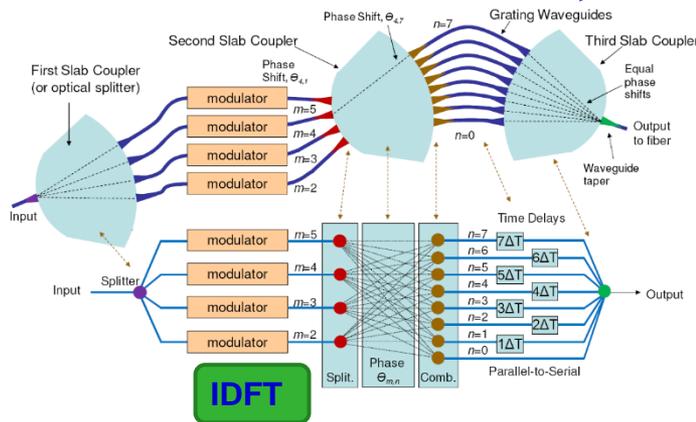
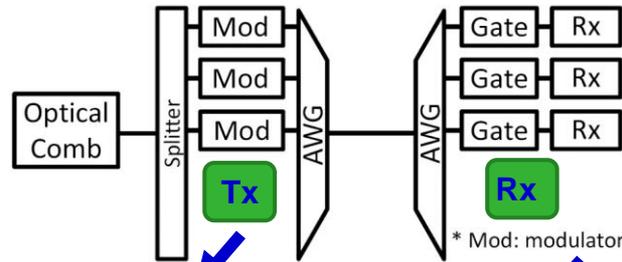
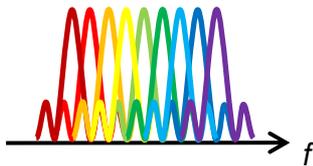


Optical shaping

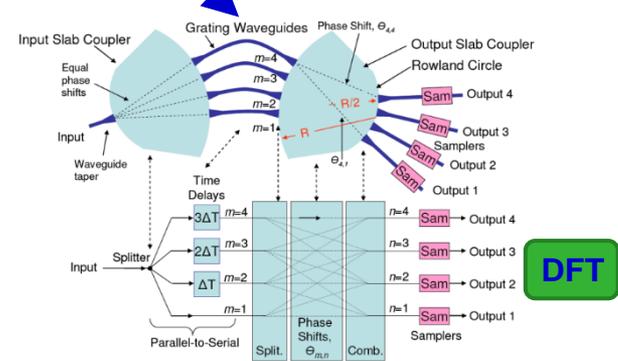
- Wide spectral range
- Slower modulator
- Passive optical processor

All-optical OFDM

Super-channel spectrum



IDFT



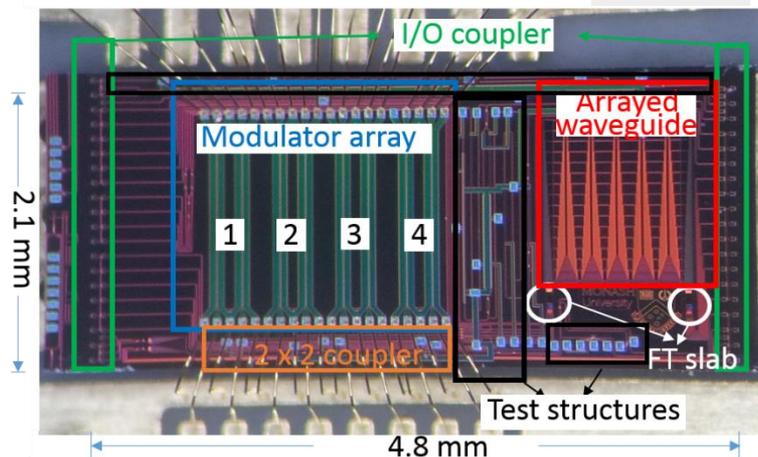
DFT

Arthur. J. Lowery and Liang B. Du, *Opt. Exp.* 19(17), 15696 (2011).
 Arthur. J. Lowery, *Opt. Exp.* 18(13), 14129 (2010).

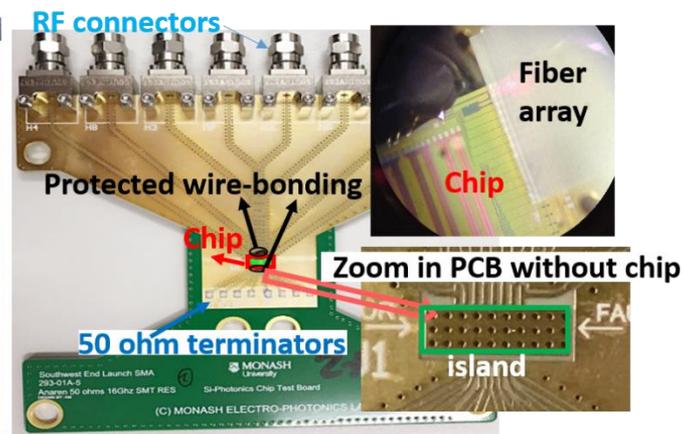
optical OFDM transmitter

(a) Photograph of OFDM Tx

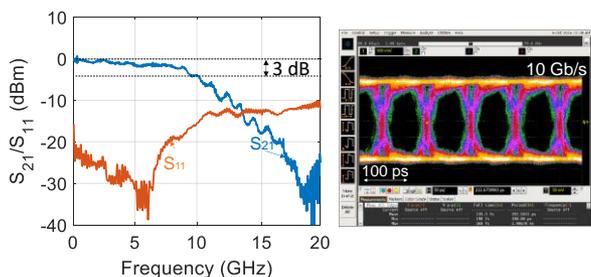
Silicon



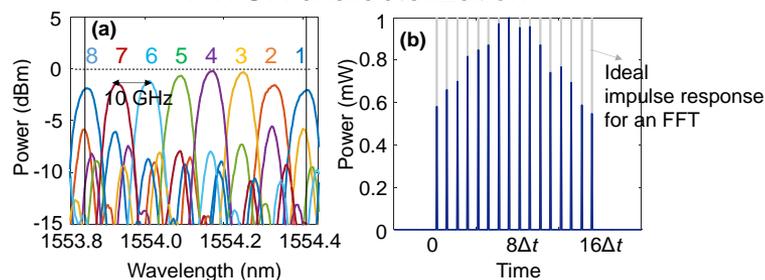
(b) Photograph of packaged OFDM Tx



Modulator characterization



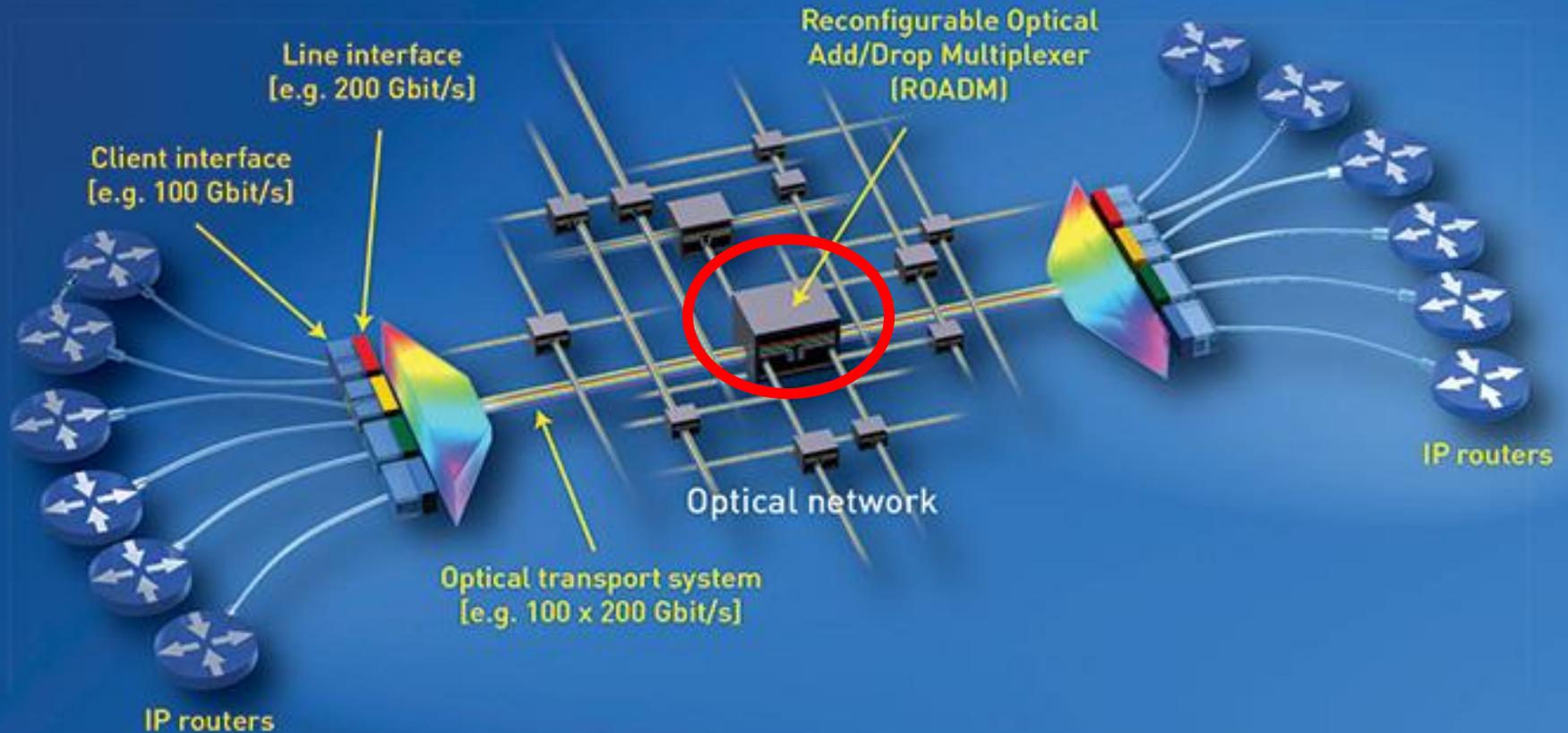
AWGR characterization



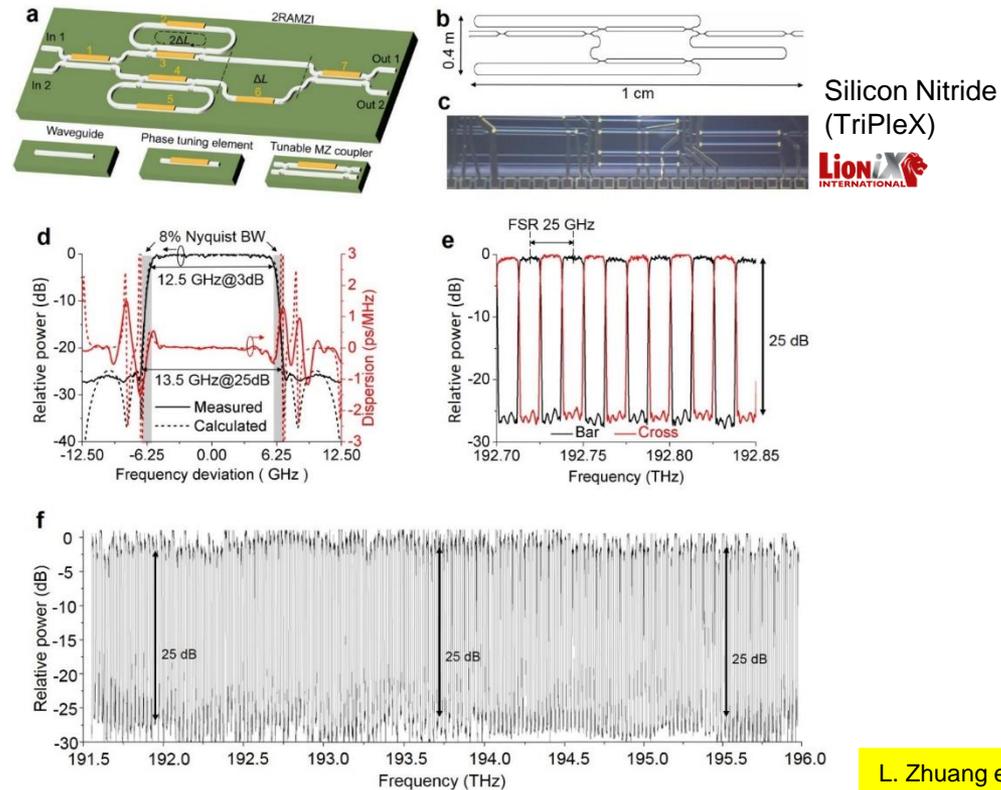
Y. Xie et al., OFC2017, W2A.9

Nyquist-WDM-superchannel ROADM

Key components of an optical transport network



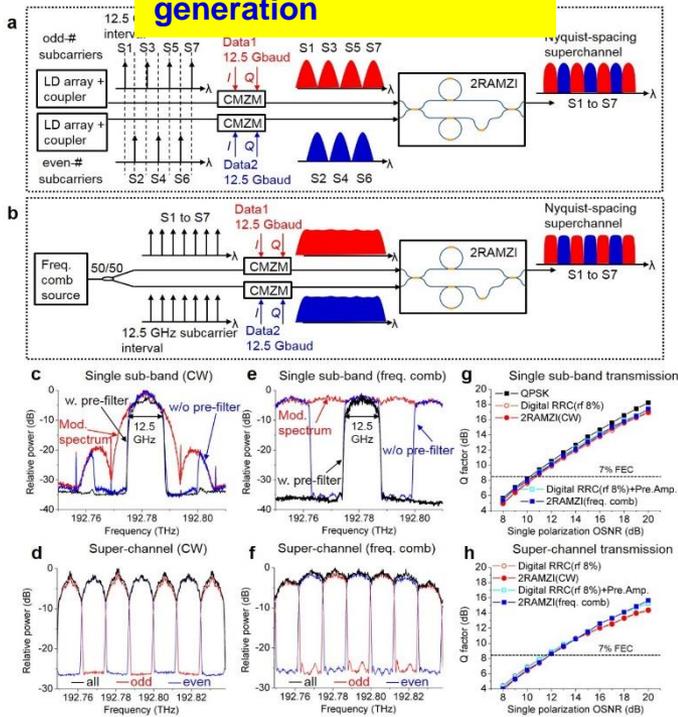
Nyquist WDM superchannel



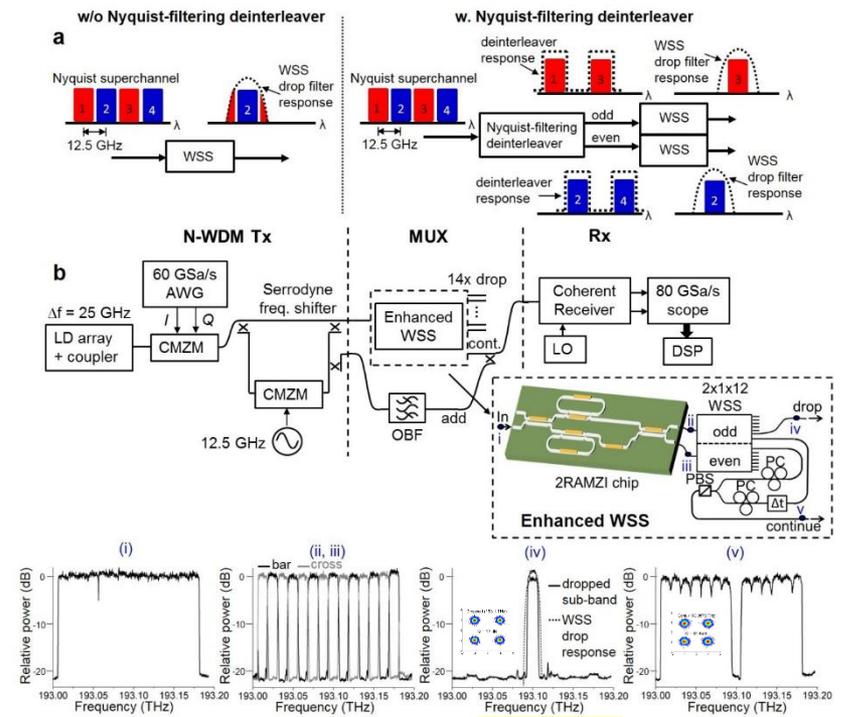
L. Zhuang et al., Opt. Express
21(7), 9167, 2016

Nyquist WDM superchannel

Superchannel generation



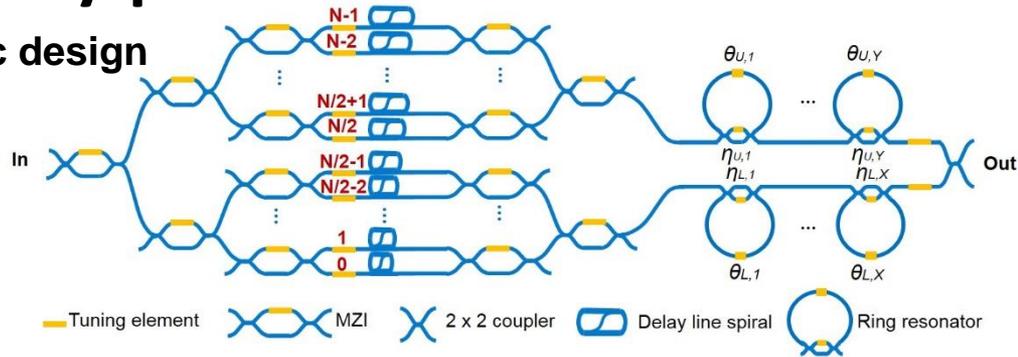
Superchannel ROADM



12.5 GHz

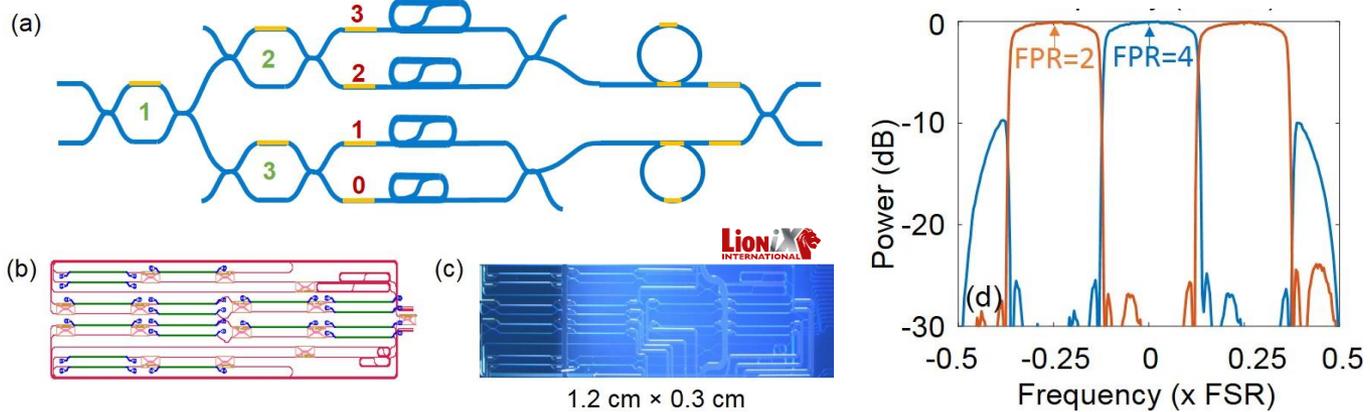
FSR-variable Nyquist WDM filter

Generic design

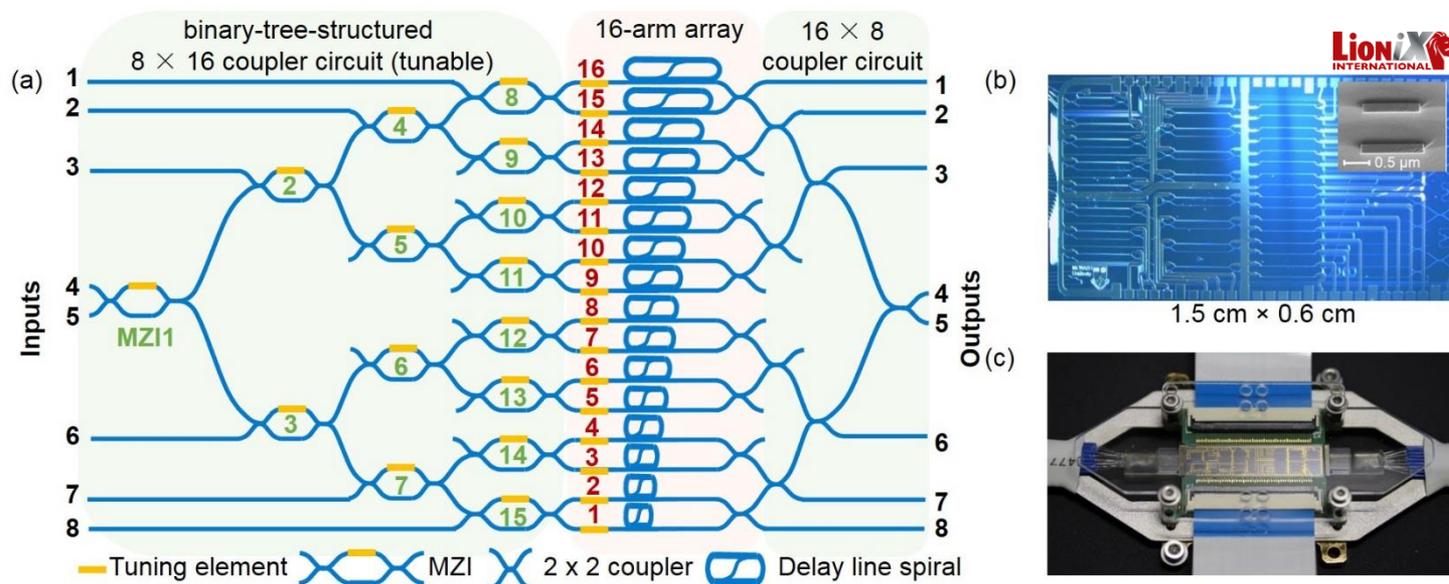


Y. Xie et al., JLT 36(13), 2619, 2018

Proof-of-concept demonstration (4 delay arms)



Picosecond pulse processing using a THz-BW reconfigurable chip



Nyquist pulse generation;

- 40 GHz bandwidth near rectangular spectrum, and sinc pulse with width of 25 ps

Clock rate multiplication;

- 10 Gpulse/s to 20 Gpulse/s or 40 Gpulse/s

Arbitrary waveform generation;

- Ramps, steps, sinc, square, random binary bit pattern

Tunable delays;

- 0-100 ps delays

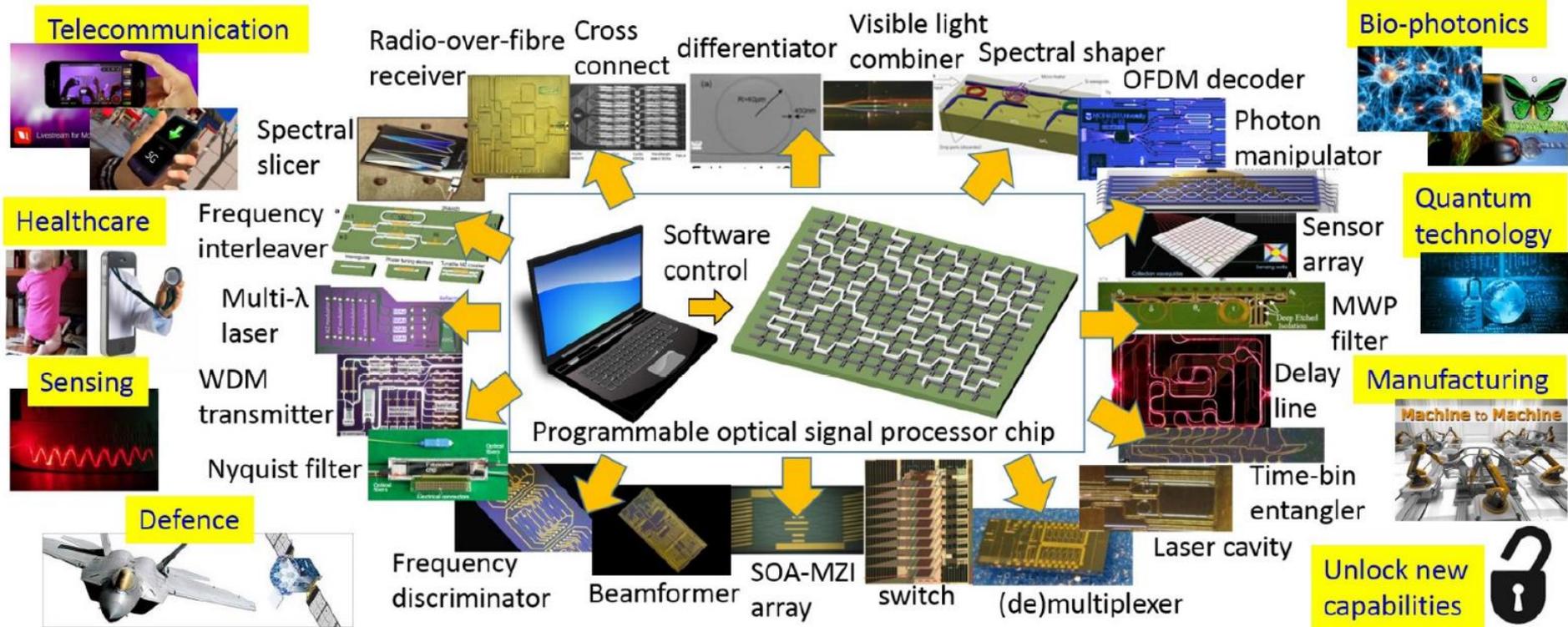
Multi-path combining;

- 10 Gpulse/s to 40 Gpulse/s

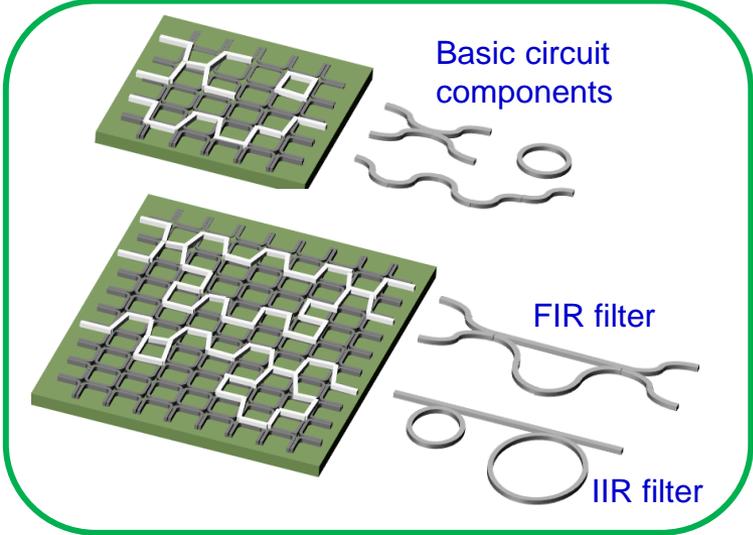
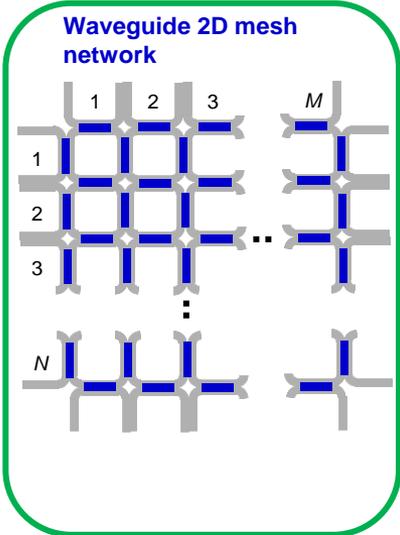
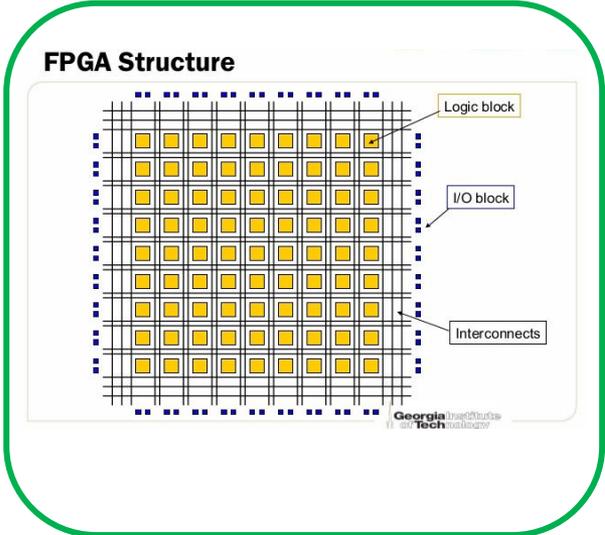
Nanophotonics -2017-0113

Programmable photonics

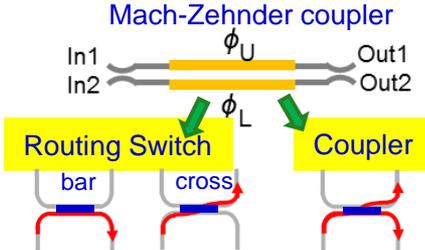
General-purpose signal processor



Programmable waveguide 2D mesh network



- Waveguide
- Mach-Zehnder coupler
- Phase tuning element
- Light propagation



$\Delta\tau$

In1 In2 Out1 Out2

ϕ_U

ϕ_L

Phase **Amplitude** **Delay**

$$C_{11} = -C_{22} = -j \exp\left(\frac{\phi_U + \phi_L}{2}\right) \sin\left(\frac{\phi_U - \phi_L}{2}\right) \exp(j2\pi f \Delta\tau)$$

$$C_{12} = C_{21} = -j \exp\left(\frac{\phi_U + \phi_L}{2}\right) \cos\left(\frac{\phi_U - \phi_L}{2}\right) \exp(j2\pi f \Delta\tau)$$

Mesh lattice

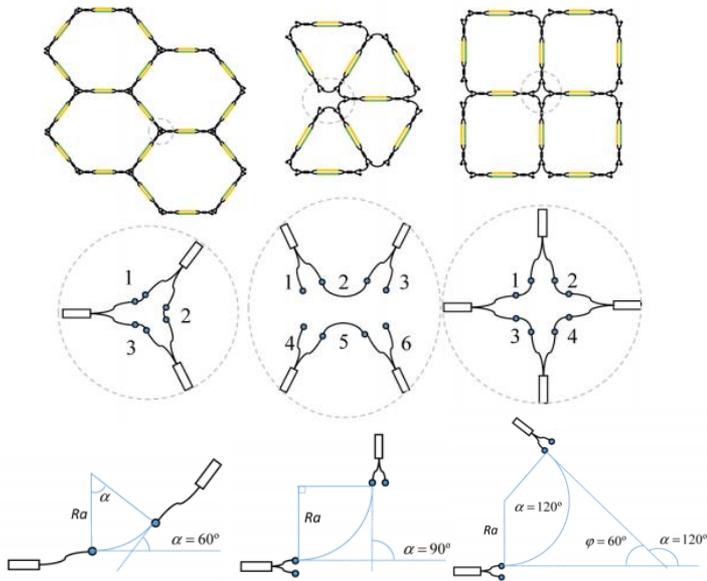
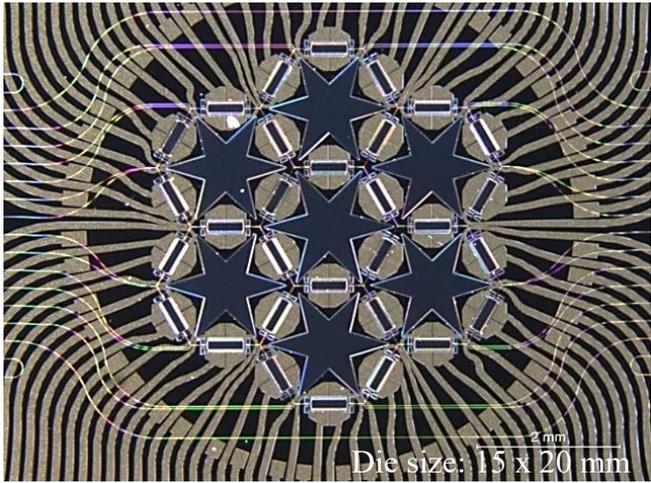


Figure of Merit	Triangular	Square	Hexagonal
ORR cavity spatial tuning resolution step in BUL units (the lower the better)	3	4	2* The first step has a resolution of 6
MZI arm imbalance spatial tuning resolution step in BUL units (the lower the better)	3	4	2
ORR reconfiguration performance (the higher the better) (for X = 25 BUL)	8	6	9
MZI reconfiguration performance (for X = 25 BUL)	8	6	12
Switching elements per unit area (the lower the better for a fixed value of reconfiguration performance)	3.96	2.40	1.52
Replication Ratio for ORR structures up to 16 BUL cavity length (the higher the better).	1	2.68	1.31
Replication Ratio for MZI structures up to 12 BUL cavity length (the higher the better).	1	3	1.31
Laccess/Laccess square % for a fixed Ra (the lower the better)	+ 33.33%	+ 0.00%	33.33%
Ra/Rasquare % for a fixed BUL (the higher the better)	25.00%	+ 0.00%	+ 50.00%

D. Pérez et al., Opt. Express
24(11), 12093, 2016

Field programmable photonic array: reconfigurable core

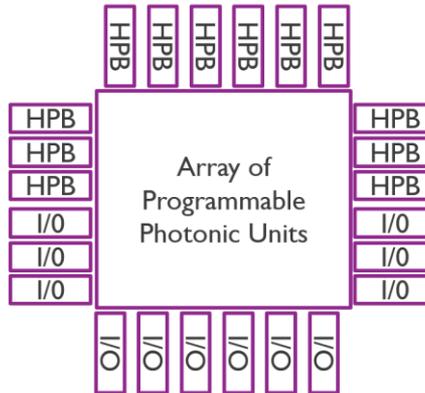


Die size: 15 x 20 mm

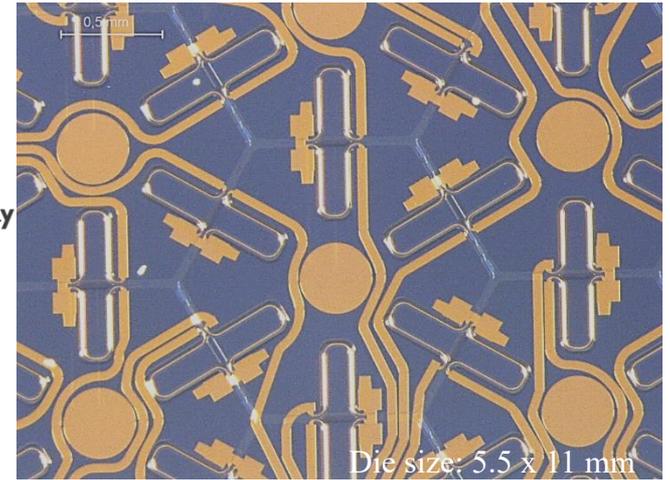
BUL= 975 μm

$n_g = 4.18$

Field-Programmable Photonic Array



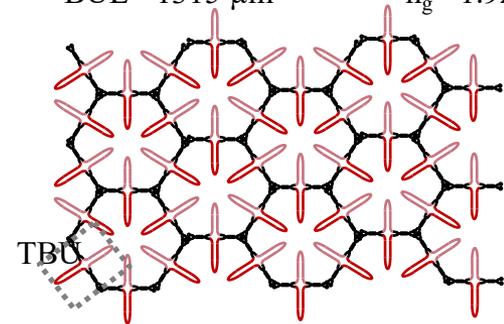
HPB High-Performance Building block
I/O Input/output ports



Die size: 5.5 x 11 mm

BUL= 1315 μm

$n_g = 1.92$



TBU

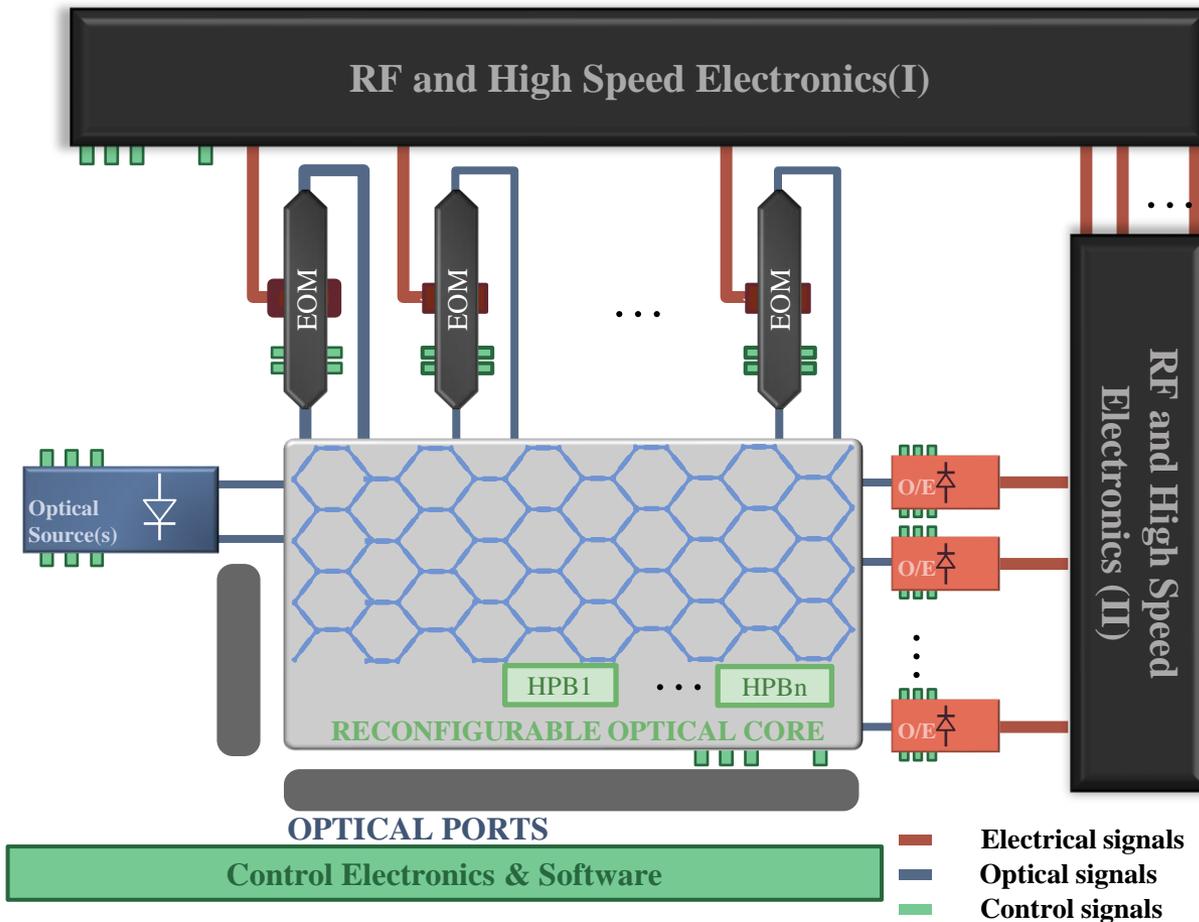


TBU

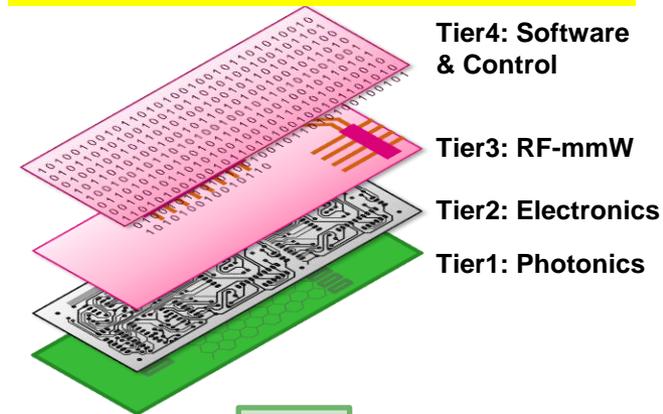


D. Pérez, et al., "Multipurpose silicon photonics signal processor core," Nat. Comms, 8, 636, (2017).

Future perspective



D. Pérez, I. Gasulla, J. Capmany, "Field-programmable photonic arrays " Optics Express, Vol. 26, no. 21, p.27265, (2017)



HPB

High-Performance Building Blocks:

- Delay line array
- Narrowband High-Q filters
- Amplification
- MUX/DEMUX
- Electro-optic Modulators
- Photodetectors
- Optical sources
- ...

Future hardware platform



40nm CMOS 4x20Gb/s Transceiver

imec Silicon Photonics Chip 40nm Foundry CMOS Chip

4x 25G Ge PD array DWDM Filter Fiber Coupler 4x 25G Ring Modulator Array 1.5mm

4x20G TIA array 4x20G Driver array

imec SI Photonics Chip Single-Mode Fiber Array 40nm Foundry CMOS Chip

imec

28nm CMOS 50Gb/s Transmitter

SiPs die with ring modulator array

Fiber in Wires Wires Fiber out

Polarization controller Tunable Laser (128Bm) PPG + MUX 54 GHz

EDFA (dB) Optical Filter Sampling Oscilloscope 40GHz BW

470Hz - 100 GHz probe

LETTER doi:10.1038/nature16454

Single-chip microprocessor that communicates directly using light

Chen Sun^{1,2*}, Mark T. Wade^{3*}, Yunsup Lee^{4*}, Jason S. Orcutt^{1,2*}, Luca Alloatti¹, Michael S. Georgas¹, Andrew S. Waterman¹, Jeffrey M. Shamir^{1,2}, Rimas R. Arviniene¹, Sen Lin¹, Benjamin R. Moss¹, Rajesh Kumar¹, Fabio Fraranzo¹, Amir H. Arabadzisz¹, Henry M. Cook¹, Albert J. Ou¹, Jonathan C. Leu¹, Yu-Hsin Chen¹, Krste Asanovic¹, Rajeev J. Ram², Miloš A. Popović¹ & Vladimir M. Stojanović¹

Figure 1 | The electro-optic system on a chip. a, Chip photos of the transmitter and receiver banks are shown. **b**, Multi-layer view of the transmitter and receiver banks. **c**, Schematic diagram of the transmitter and receiver banks. **d**, Schematic diagram of the transmitter and receiver banks. **e**, Schematic diagram of the transmitter and receiver banks. **f**, Schematic diagram of the transmitter and receiver banks. **g**, Schematic diagram of the transmitter and receiver banks. **h**, Schematic diagram of the transmitter and receiver banks. **i**, Schematic diagram of the transmitter and receiver banks. **j**, Schematic diagram of the transmitter and receiver banks. **k**, Schematic diagram of the transmitter and receiver banks. **l**, Schematic diagram of the transmitter and receiver banks. **m**, Schematic diagram of the transmitter and receiver banks. **n**, Schematic diagram of the transmitter and receiver banks. **o**, Schematic diagram of the transmitter and receiver banks. **p**, Schematic diagram of the transmitter and receiver banks. **q**, Schematic diagram of the transmitter and receiver banks. **r**, Schematic diagram of the transmitter and receiver banks. **s**, Schematic diagram of the transmitter and receiver banks. **t**, Schematic diagram of the transmitter and receiver banks. **u**, Schematic diagram of the transmitter and receiver banks. **v**, Schematic diagram of the transmitter and receiver banks. **w**, Schematic diagram of the transmitter and receiver banks. **x**, Schematic diagram of the transmitter and receiver banks. **y**, Schematic diagram of the transmitter and receiver banks. **z**, Schematic diagram of the transmitter and receiver banks.

Berkeley UNIVERSITY OF CALIFORNIA

Conclusion

- Combining signal processing in both electrical and optical domain brings clear benefit for transmission capacity and power efficiency
- Field programmability increases the potential for applications of optical signal processors
- Advancing in hybrid electronics-photonics integration technologies promise a robust hardware platform

Thank you for your attention

leimeng.zhuang@ieee.org