

A person wearing a white lab coat and gloves is holding a large, rectangular, colorful chip or wafer. The chip has a complex, grid-like pattern of small, colorful components (red, green, blue, yellow) and is being held up to the light. The background is a blurred laboratory setting.

DE CHIP VAN DE TOEKOMST: WAT IS DE ROL VAN NEDERLAND EN EUROPA?

Bart Smolders, Scientific Director Casimir Institute

Semiconductor eco system

Erteilt auf Grund des Ersten Überleitungsgesetzes vom 8. Juli 1949

(WIGBl. S. 175)

BUNDESREPUBLIK DEUTSCHLAND



AUSGEGEBEN AM
5. NOVEMBER 1959

DEUTSCHES PATENTAMT

PATENTSCHRIFT

Nr. 972 909

KLASSE 21g GRUPPE 1102

INTERNAT. KLASSE H 011

N 1999 I III c / 21 g

Pieter Johannes Wilhelmus Jochems und Leonard Johan Tummers,
Eindhoven (Niederlande)
sind als Erfinder genannt worden

N. V. Philips' Gloeilampenfabrieken, Eindhoven (Niederlande)

Halbleiteranordnung unter Verwendung eines Halbleiterkörpers,
auf dem mindestens zwei gleichrichtende Elektroden
und eine weitere Elektrode angebracht sind,
und Einrichtung mit einer solchen Halbleiteranordnung

Patentiert im Gebiet der Bundesrepublik Deutschland vom 24. September 1950 an

Patentanmeldung bekanntgemacht am 26. April 1951 .

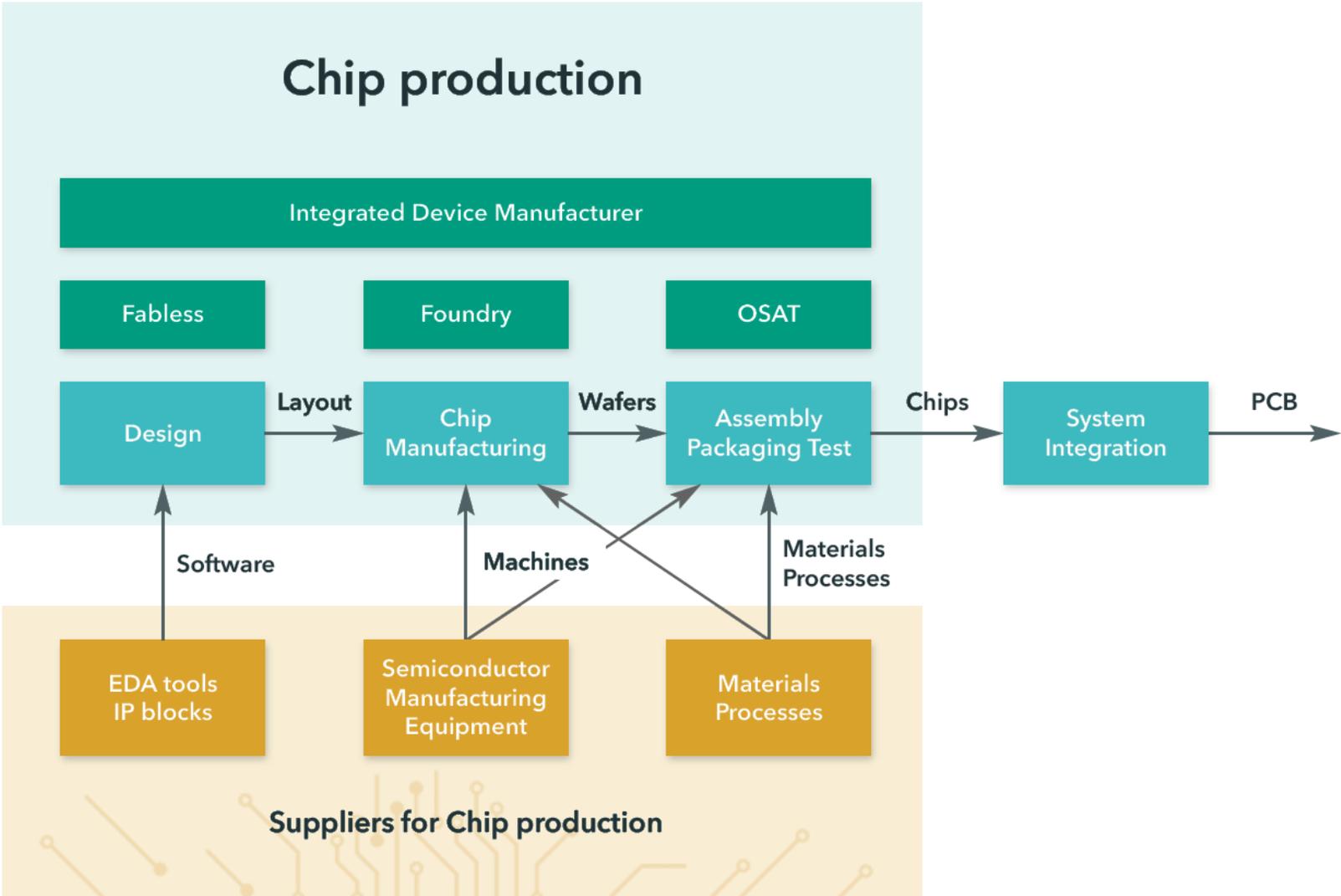
Patenterteilung bekanntgemacht am 15. Oktober 1959

Die Priorität der Anmeldungen in den Niederlanden vom 28. September und 7. Oktober 1949

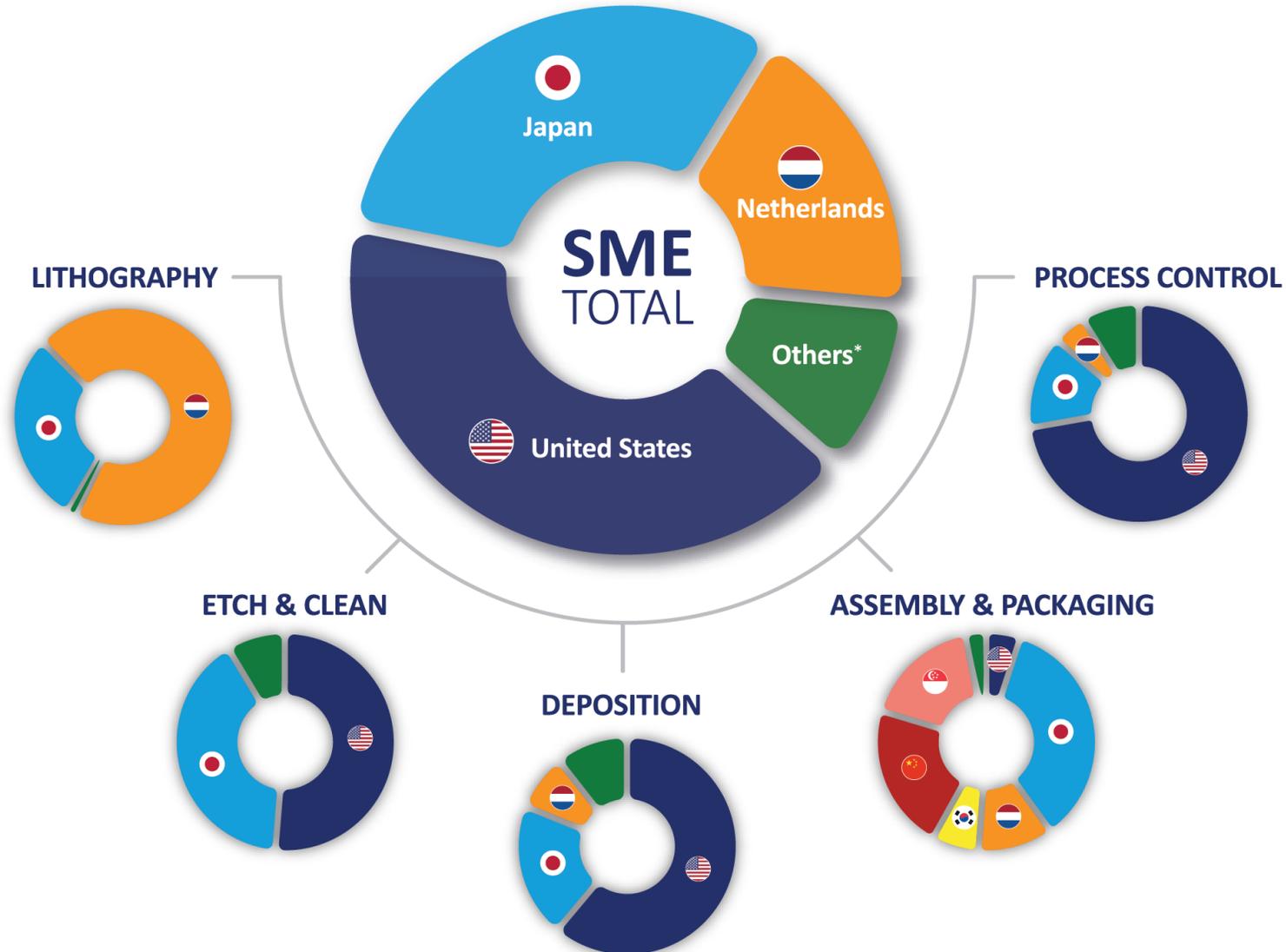
ist in Anspruch genommen

Fig.6.1. Titelblad van het eerste transistoroetrooti van Philips.

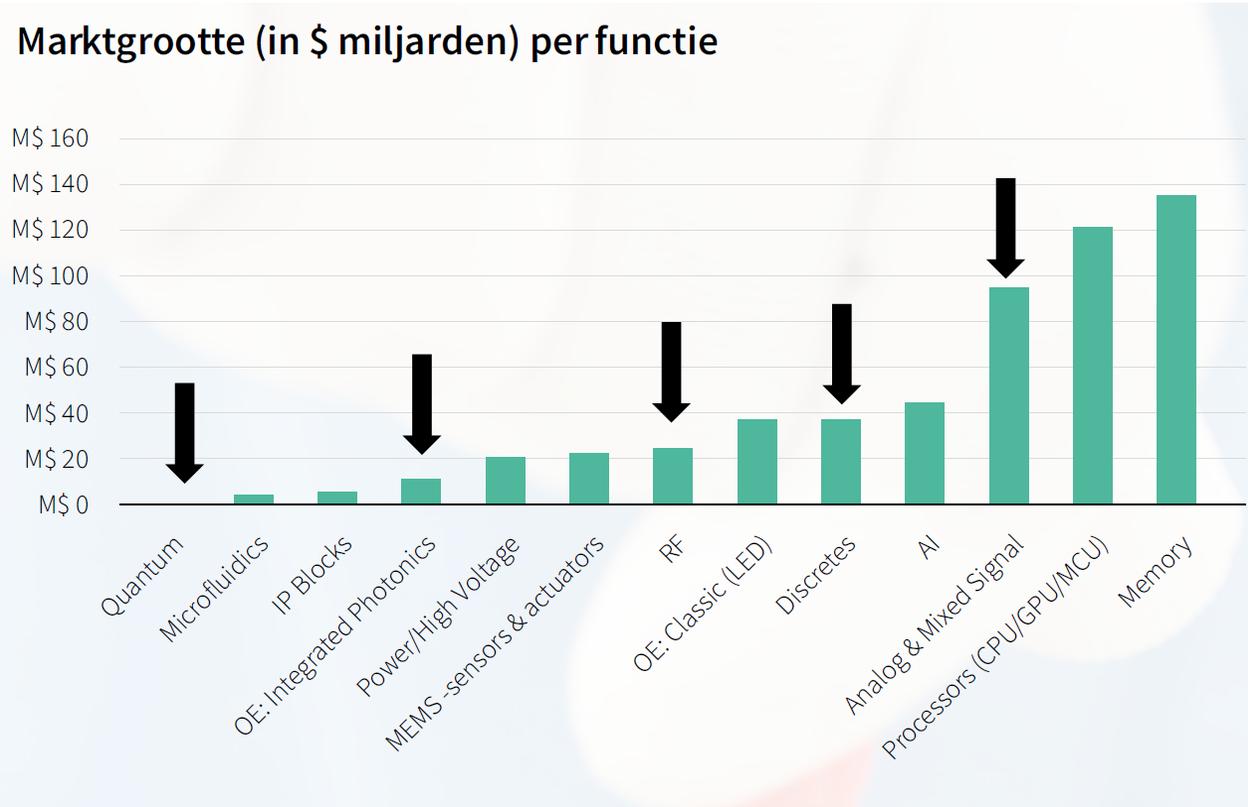
Semiconductor eco-system



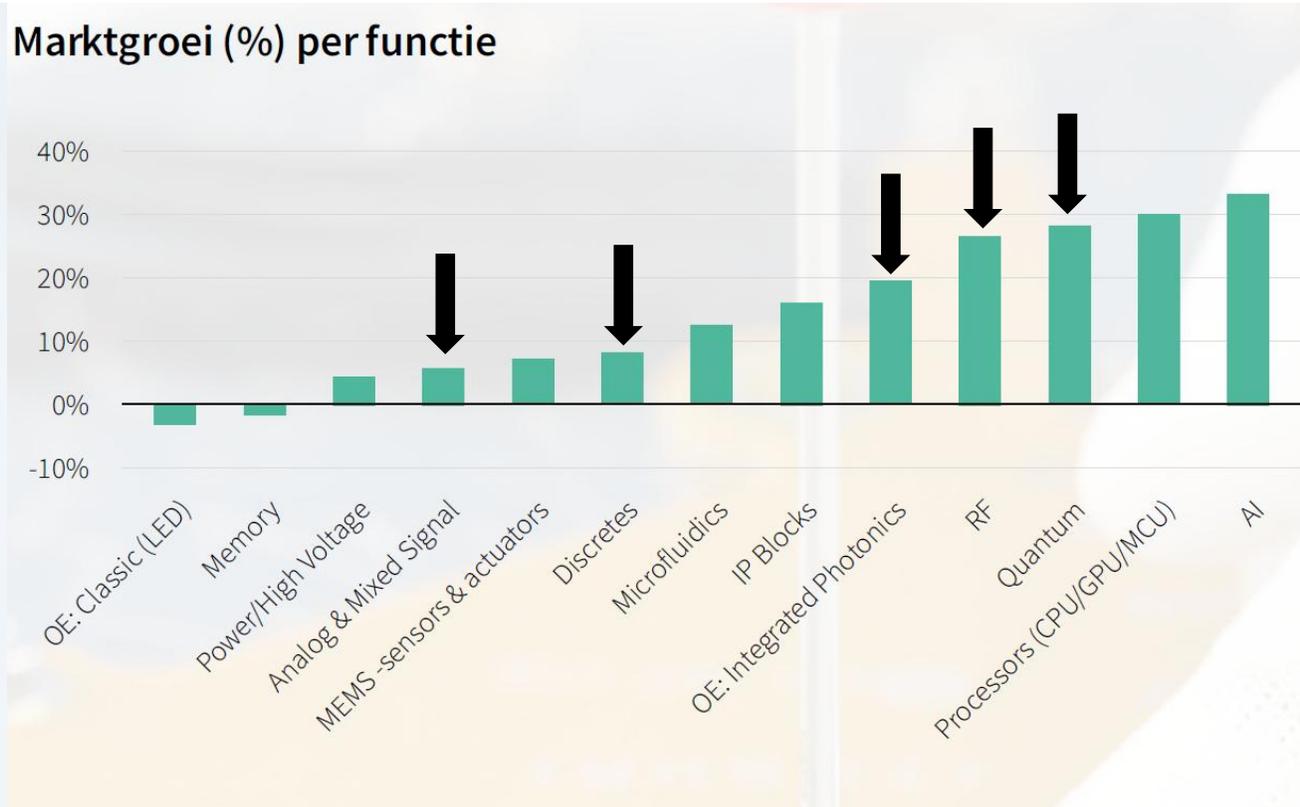
NL global player in Semiconductor Manufacturing Equipment



In Chip Design the NL/EU position is strong in some market segments



Figuur 3: Marktomvang van de verschillende chipsegmenten, Bron: Brainport marktonderzoek, mei 2024



Figuur 4: Verwachte groei per type chip, Bron: Brainport marktonderzoek, mei 2024.

Dutch semiconductor ecosystems

NL plays key role in semicon ecosystems



Our “pareltjes” in Semiconductors



How are we doing at this moment?

Strength NL

- Top 3 player worldwide in semiconductor manufacturing equipment
- Chip design for RF and Analog/Mixed-Signal

Weaknesses EU/NL

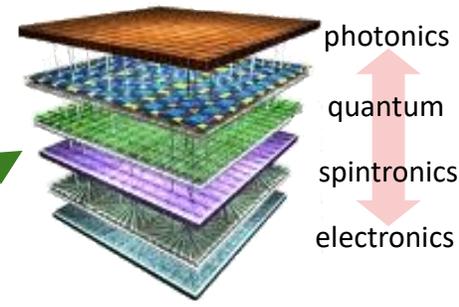
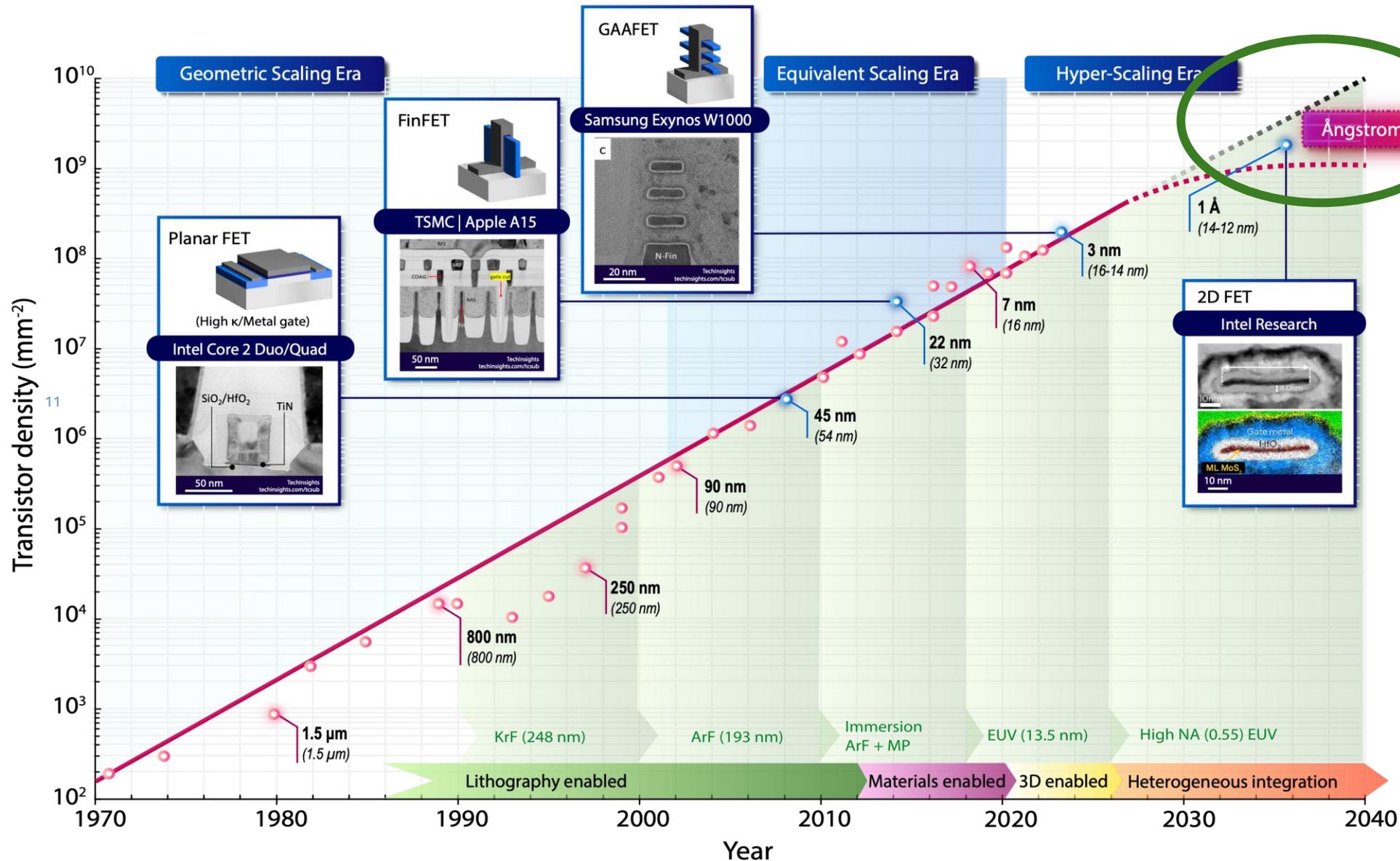
- Digital chip design (although we have unicorn Axelera AI.....)
- No fabs for advanced CMOS and packaging/test.

Opportunities EU/NL

- Heterogeneous integration, combining electronics and photonics
- Chip design to enable robotics/physical AI

What is next?

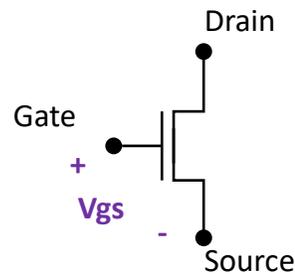
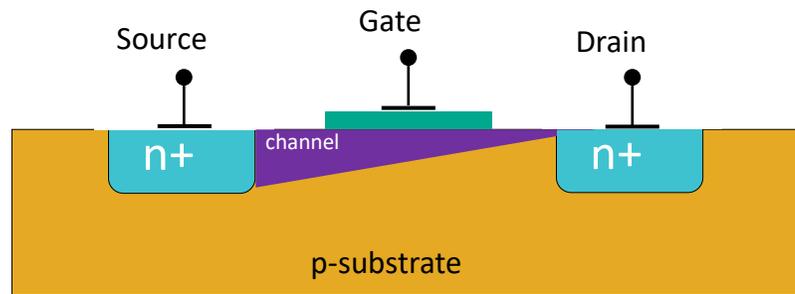
Moore's law needs new breakthroughs



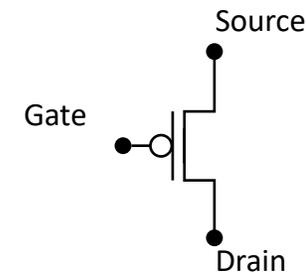
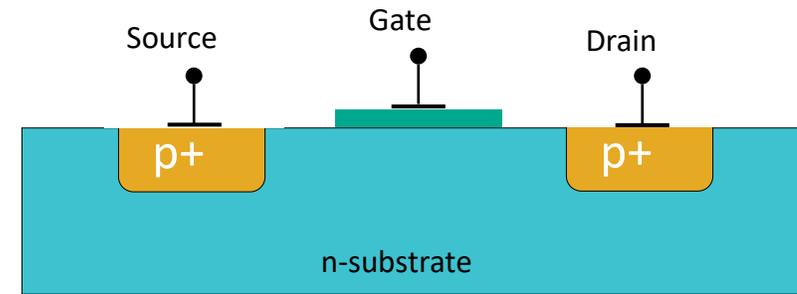
Intermezzo: What is CMOS?

What is CMOS?

- CMOS=Complementary Metal Oxide Semiconductors=NMOS+PMOS

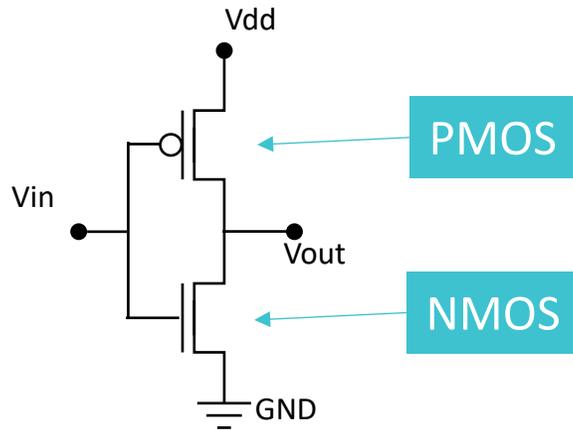


NMOS



PMOS

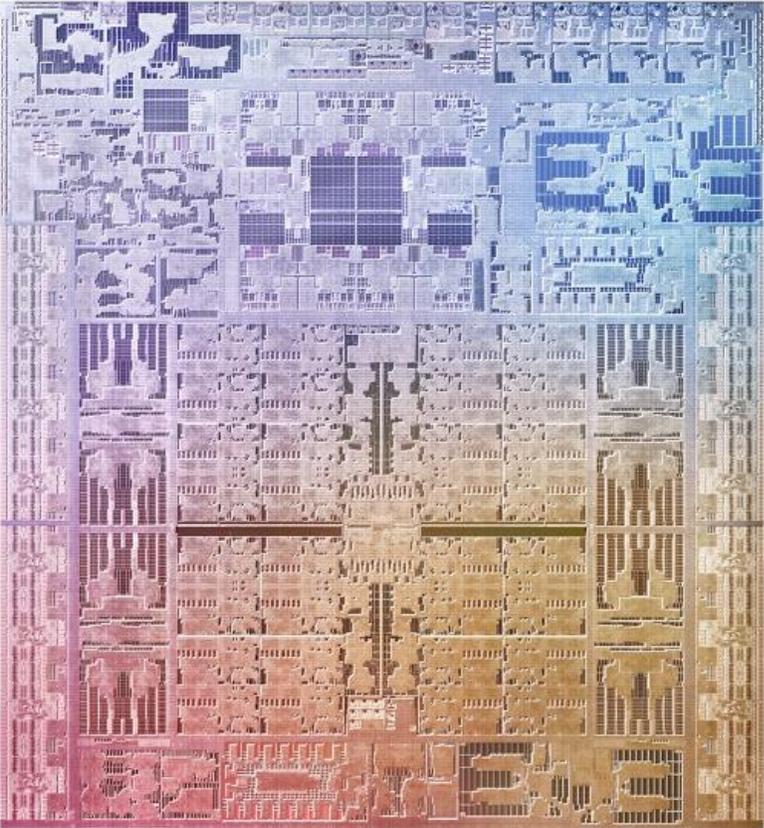
Simplest logic circuit: CMOS Inverter



CMOS Inverter

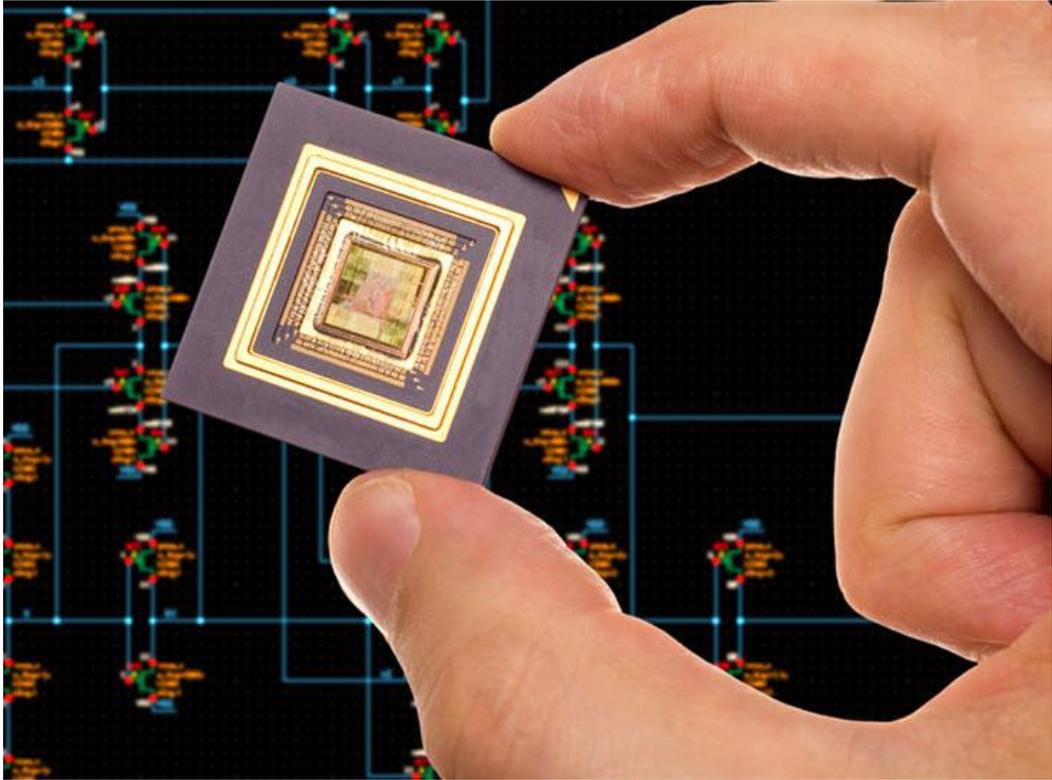
Logic input	V_{in}	V_{out}	Logic output
0	0 V	V_{dd}	1
1	V_{dd}	0 V	0

Digital Integrated Circuits



Apple M1 Max

57 Billion MOS transistors



CFET (for equivalent beyond 1nm node)

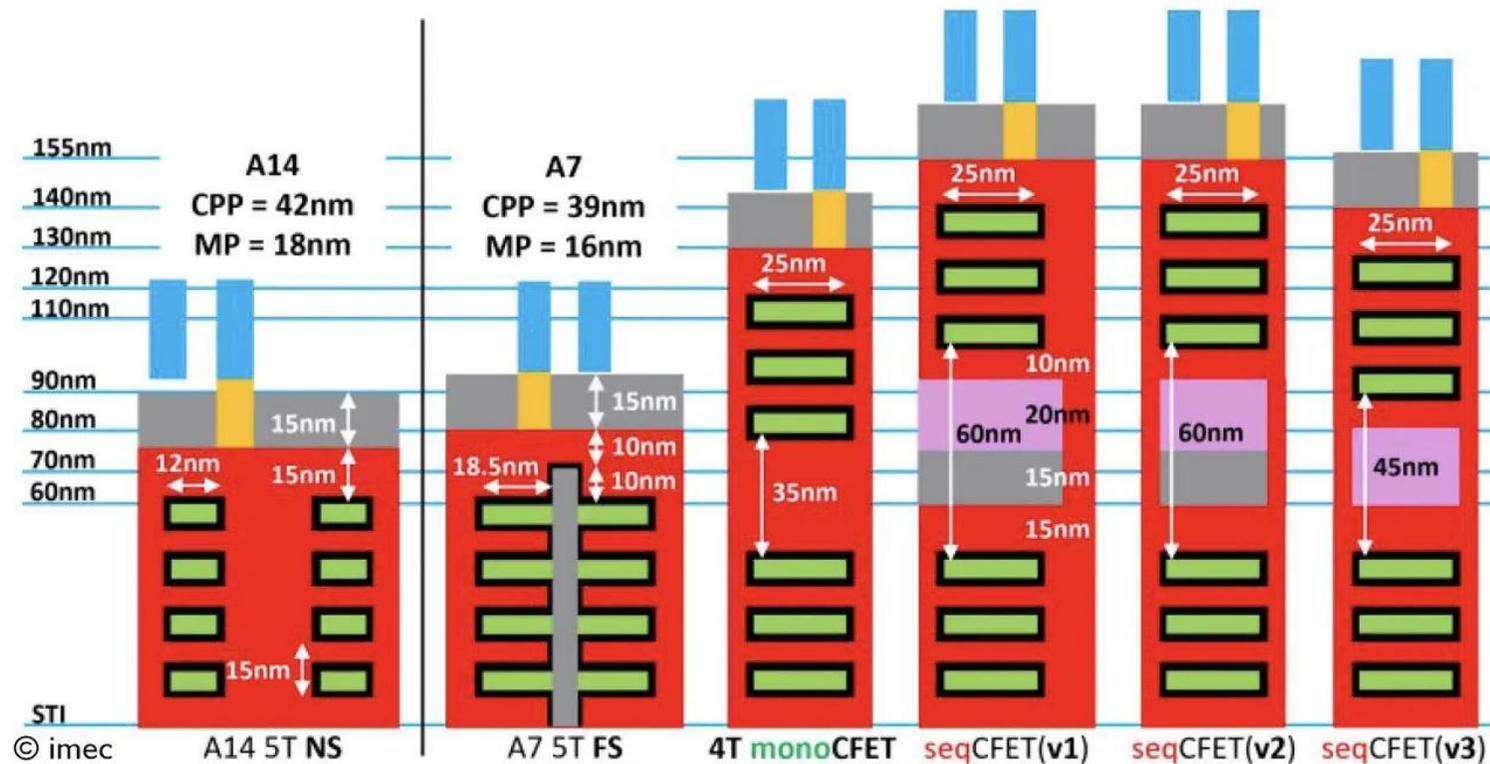
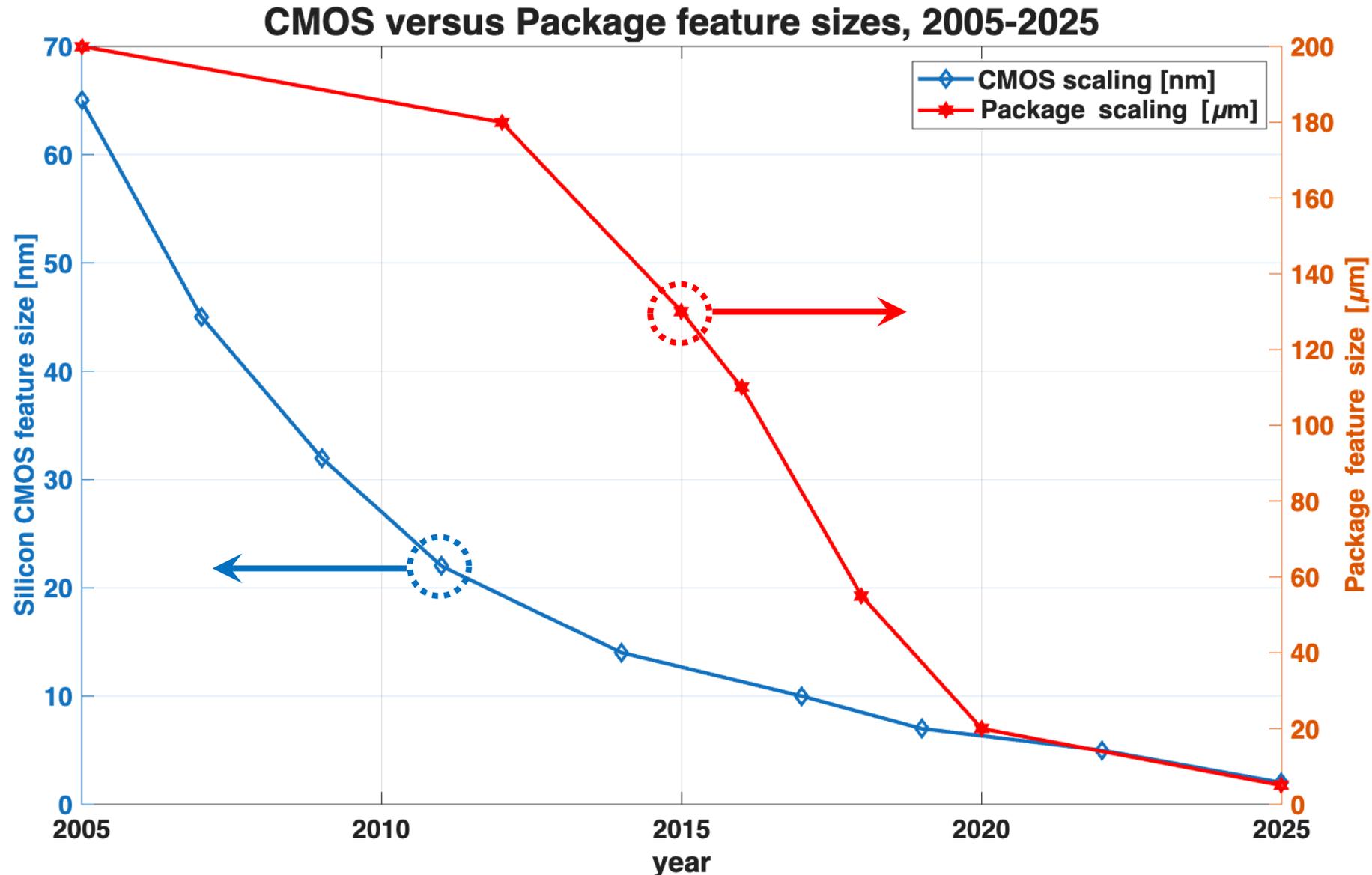


Figure 2 – Gate cross sections for nansheet (NS), forsheet (FS) and CFET (monolithic and sequential). Basic sequential CFET (=v1) is wider and taller than mono. With an optimized flow (including self-aligned gate merge (v2) and no gate cap (v3)), sequential CFET approaches monolithic CFET in terms of area consumption (also presented at VLSI 2022).

End of Intermezzo

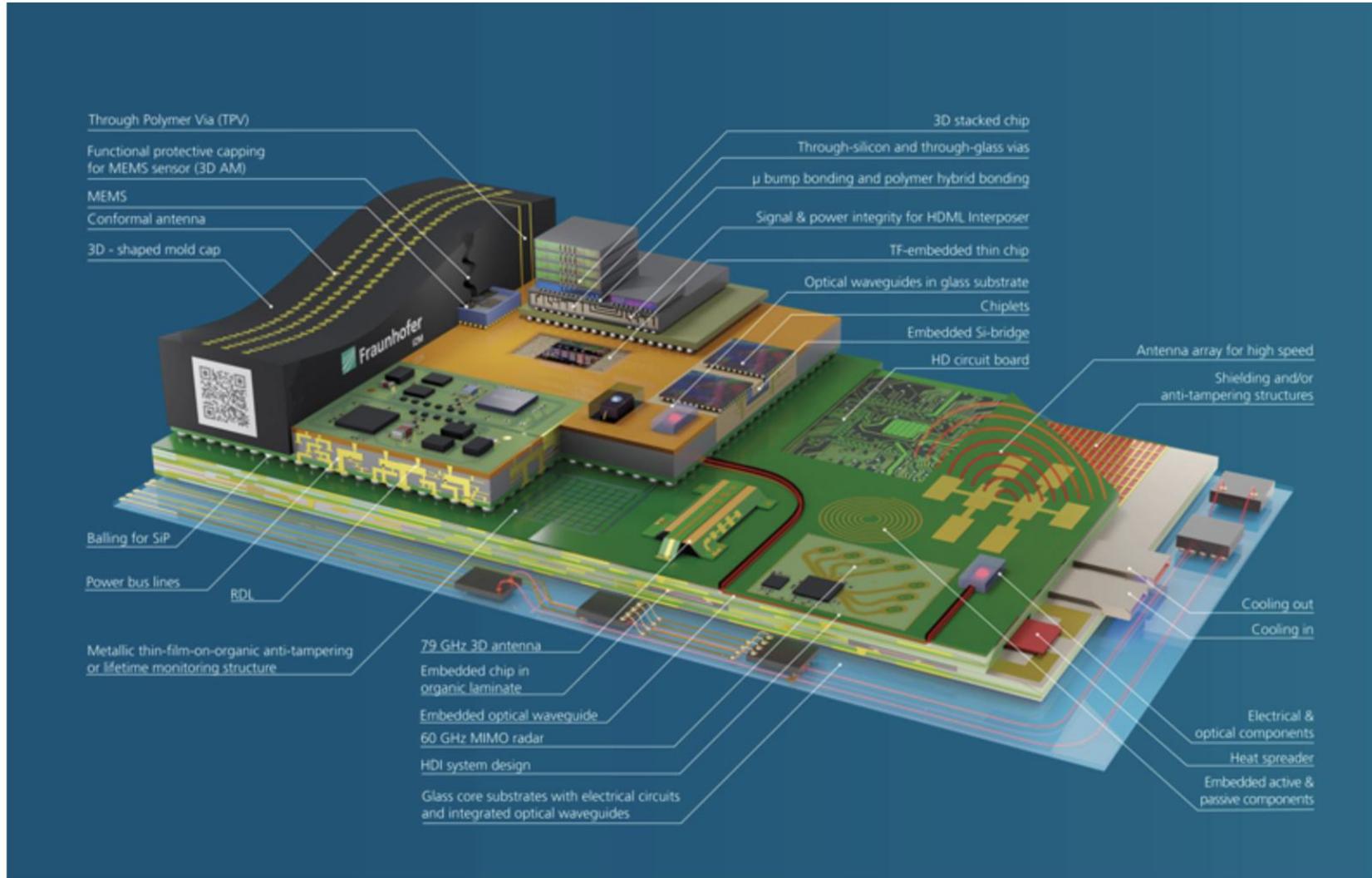
CMOS versus Advanced Packaging



[1] K. Sahoo et al, "A Review of Die-to-Die, Die-to-Substrate and Die-to-Wafer Heterogeneous Integration," *IEEE Electron Devices Reviews*, vol. 2, pp. 6-31, 2025.

[2] <https://www.imec-int.com/en/articles/introducing-2d-material-based-devices-logic-scaling-roadmap>

What is heterogeneous integration?



Vision of hetero-integration using the example of high-end performance packaging, | © Fraunhofer IZM

Why heterogeneous integration?

Drivers

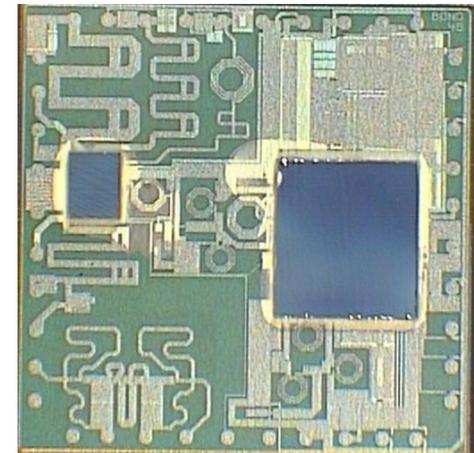
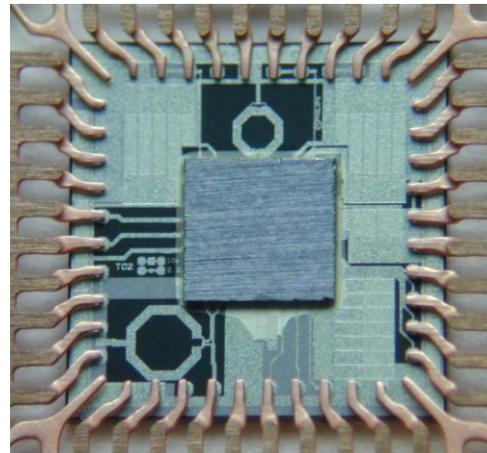
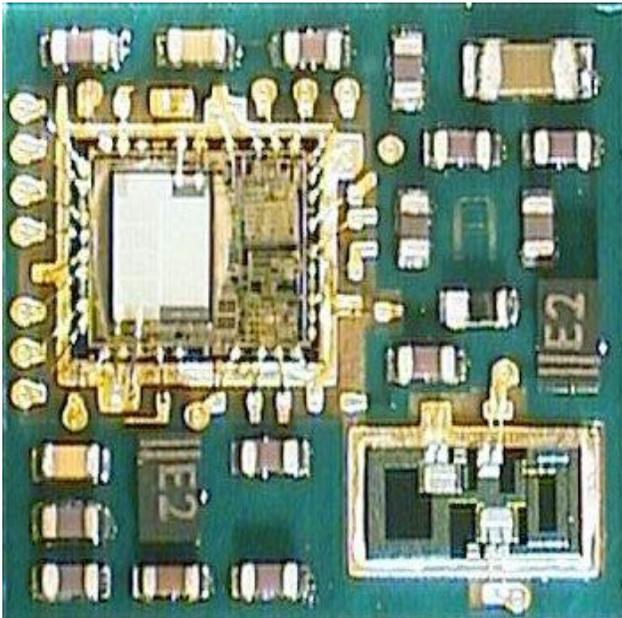
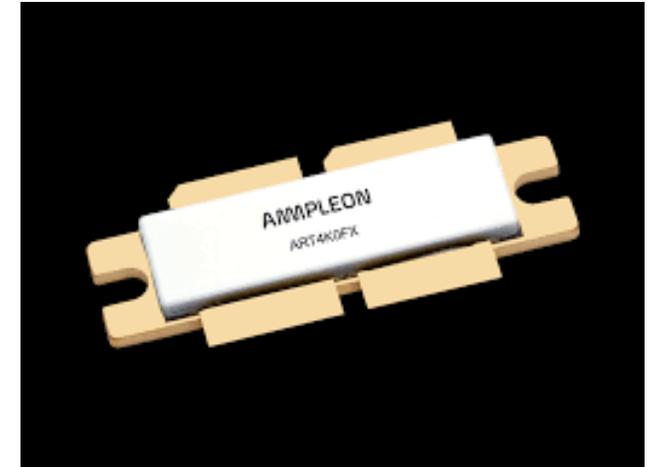
- Increase of required computing power and memory (AI and HPC)
- Increase of the number of sensors, e.g. radar and mechanical sensors
- Need to communicate larger amounts of data, either wireless (moving to higher frequencies) or wired (photonics)

This calls for a **mix of technologies**:

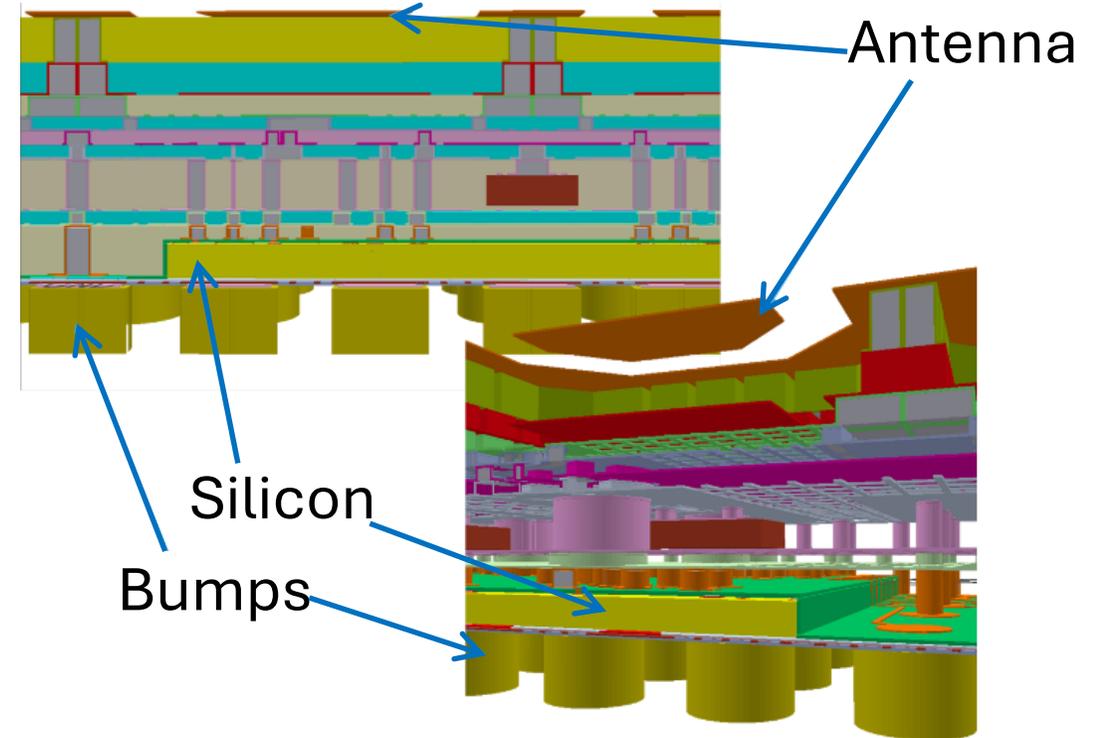
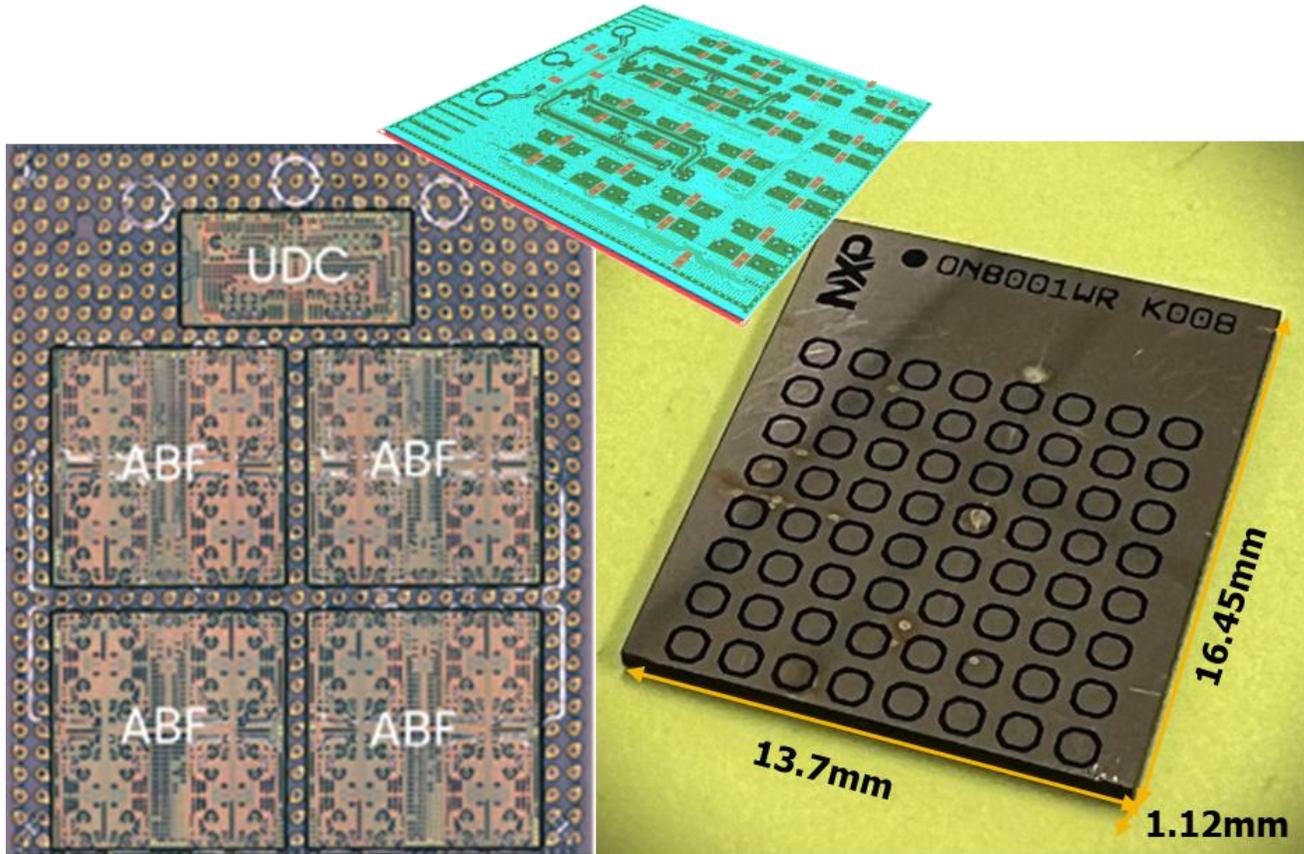
- Compute and Memory using advanced CMOS, e.g. CMOS 16nm FINFET
- RF prefers older CMOS nodes (CMOS28nm) or special technologies (InP, GaN).
- Higher frequencies (> 10 GHz) requires integration of antennas
- Photonics requires the use of InP to make active devices (lasers)

Advanced packaging is crucial for heterogenous integration to become successful

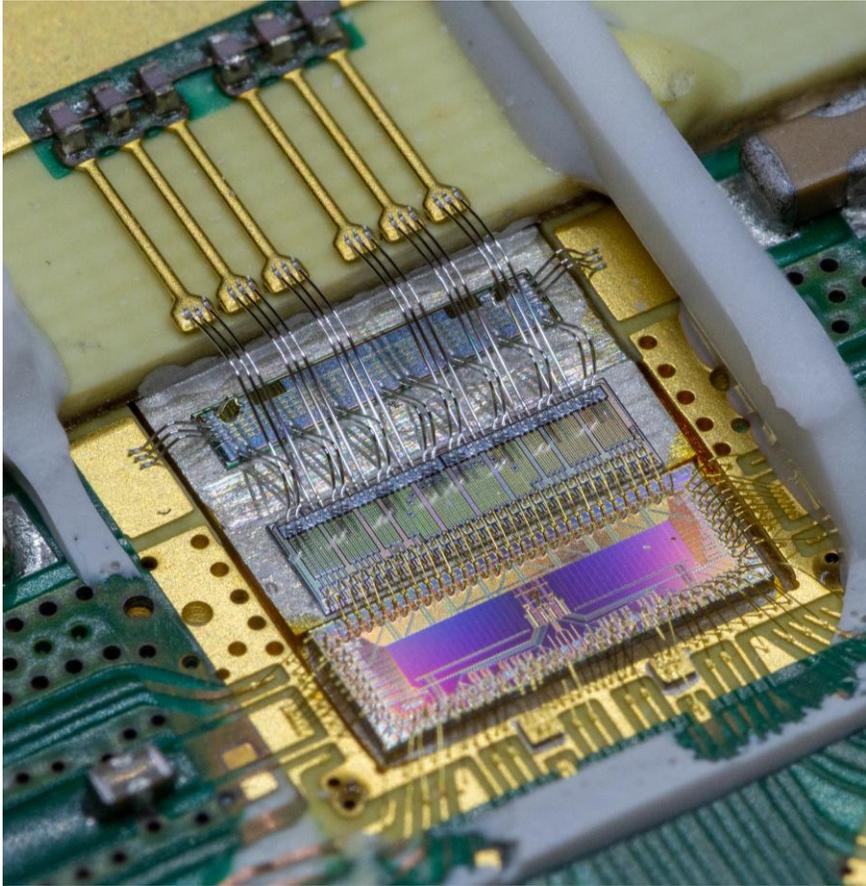
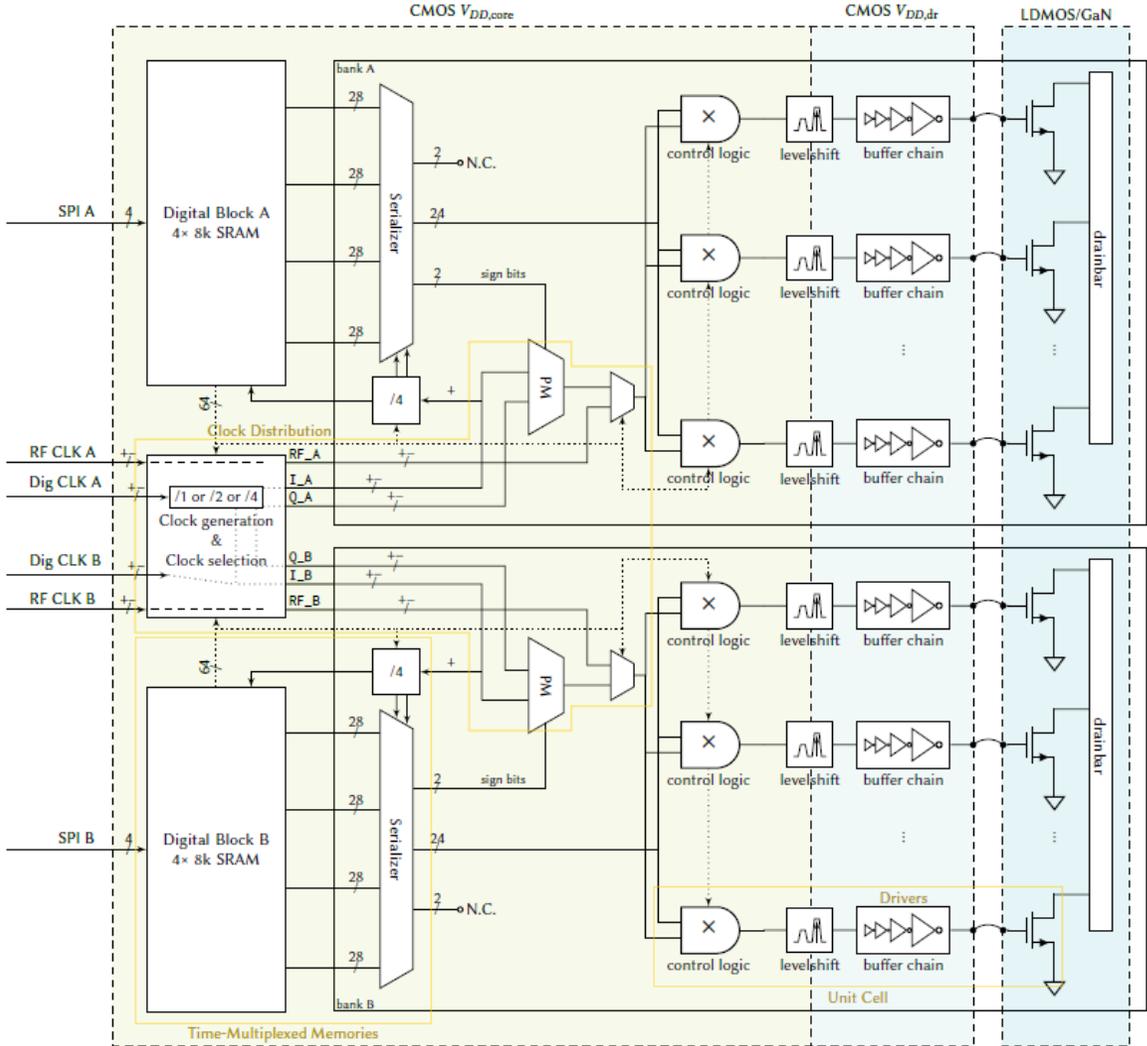
NL strong history in heterogeneous integration



100 GHz 6G Active Array Antenna in Package (AAiP)

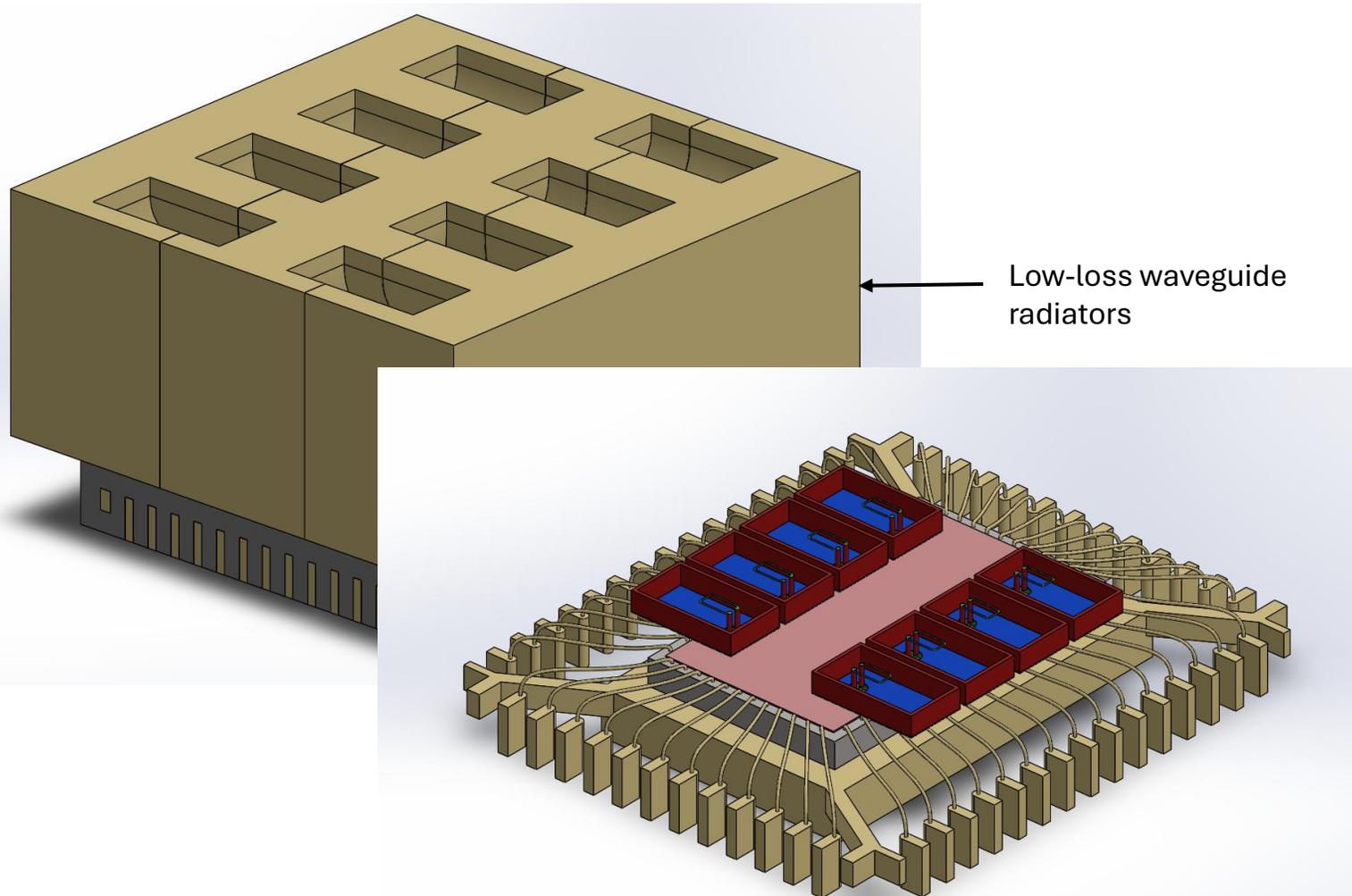


Digital power for 5G/6G wireless networks

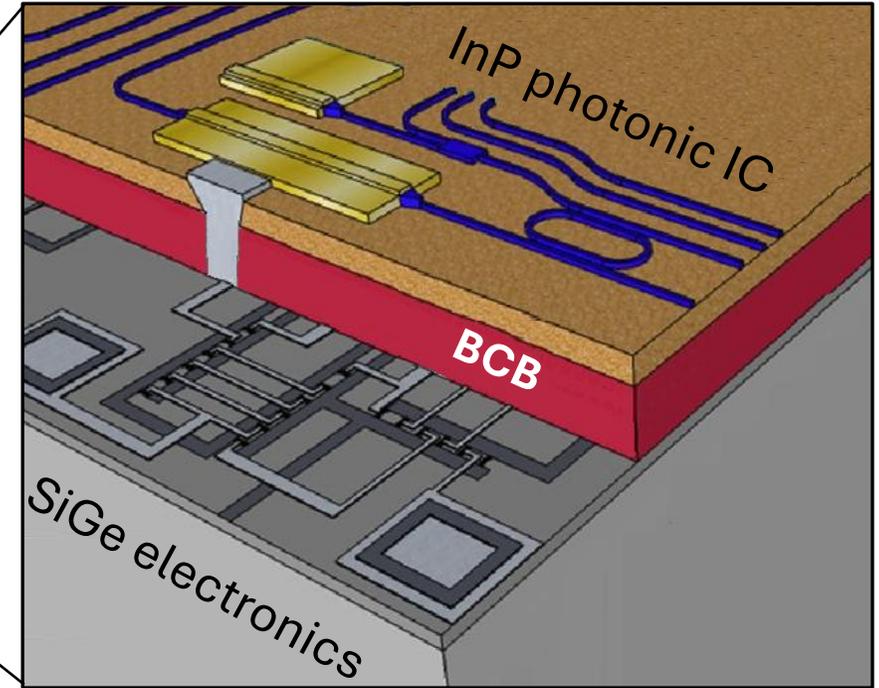
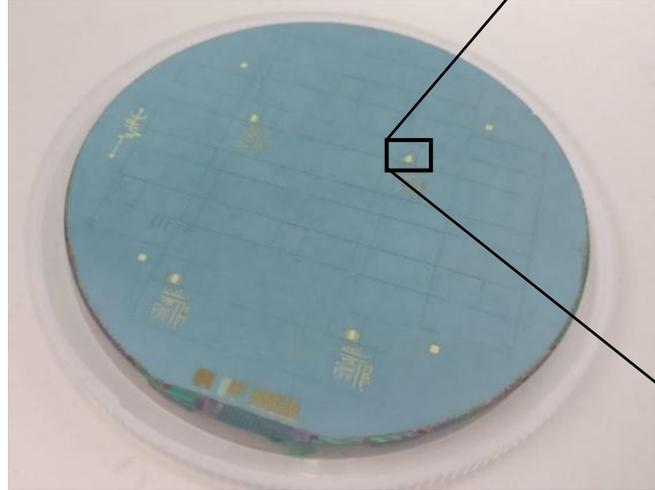
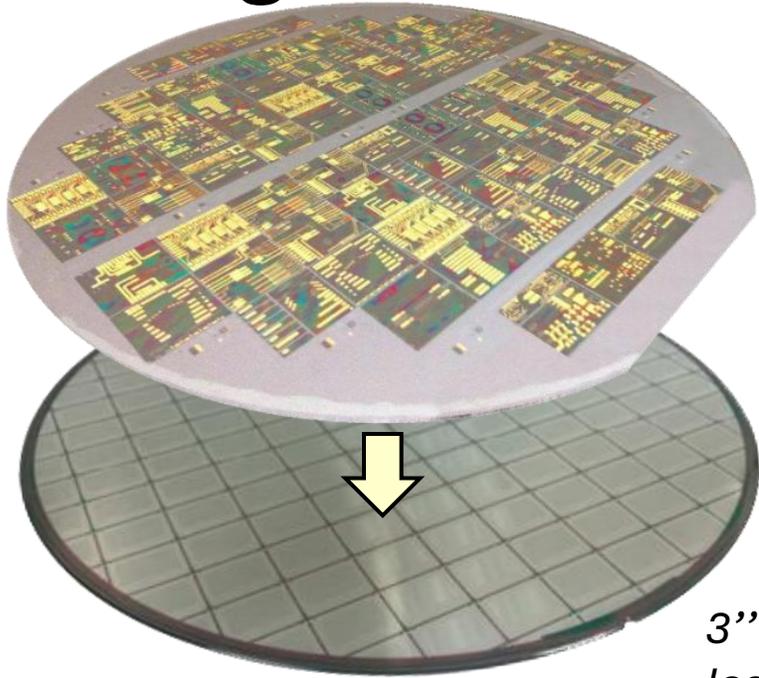


Automotive radar 77/140 GHz

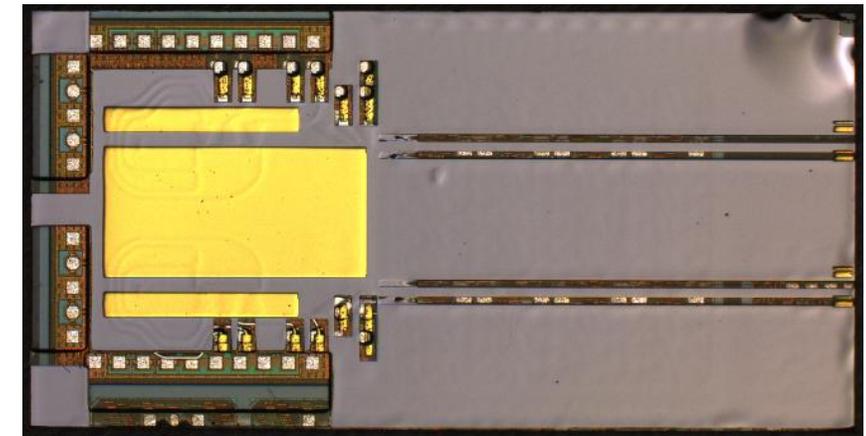
Metal-only interconnect for low-losses



Waferscale electronic-photonic integration with InP



3" InP PIC wafer from HHI bonded to laser-sawn BiCMOS wafer from NXP



Intimate co-design to remove components and parasitics
Systematically improve efficiency, speed, and information density
Using wafer scale processes



<http://wipe.jeppix.eu>



Summary

The Netherlands is a strong player in Semiconductors

- Top-3 position in semiconductor manufacturing equipment
- Strong position in RF and analog mixed signal, e.g. radar sensing

What is next?

- Moore's law is saturating and changing
- Advanced Packaging is taking off
- Offers the optimal mix of technologies, e.g. combining electronics, photonics and sensors

The Netherlands has a lot of know-how in the area of heterogeneous integration.

- Many opportunities for industry and new start-ups

Stay in touch



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